

# parallella

## **Parallella-1.x Reference Manual**

## Revision History

Version	Comments
0.13.2.13	Initial release
1.13.6.24	Updated PEC_POWER Pin outs Part Numbers Added + Document Links Changed flash to 128Mb Replaced 5V DC/USB power mux with pin header Changed power sub-system Epiphany now uses 1.8V IO voltage Added UART 2-pin header Changed license to creative common
1.13.7.27	Added UART interface back to PEC_POWER Added test points for SYS_5V and 1P0V Added 2-pin header for 5V mounting hole
14.04.15	Removed second USB port "PC connection" as supported feature No longer supporting the USB-OTG (only host mode)
14.09.09	Removed reference to reset button Remove reference to 2 <sup>nd</sup> USB port Added numerous tables, design details

## **Related Documents**

Epiphany Architecture Reference Manual:

[http://www.adapteva.com/docs/epiphany\\_arch\\_ref.pdf](http://www.adapteva.com/docs/epiphany_arch_ref.pdf)

Epiphany SDK Reference Manual:

[http://www.adapteva.com/docs/epiphany\\_sdk\\_ref.pdf](http://www.adapteva.com/docs/epiphany_sdk_ref.pdf)

Epiphany-III Datasheet:

[http://www.adapteva.com/docs/e16g301\\_datasheet.pdf](http://www.adapteva.com/docs/e16g301_datasheet.pdf)

Epiphany-IV Datasheet:

[http://www.adapteva.com/docs/e64g401\\_datasheet.pdf](http://www.adapteva.com/docs/e64g401_datasheet.pdf)

## **Software Repositories:**

Parallella Hardware and Software Repository

<https://github.com/parallella>

Epiphany SDK Software Repository

<https://github.com/adapteva>

SD Card Images:

<ftp://ftp.parallella.org>

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## 1 Overview

The Parallella board is a high performance computing platform based on a dual-core ARM-A9 Zynq System-On-Chip and Adapteva’s Epiphany multicore coprocessor. Current commercially available models:

Model	P1600	P1601	P1602
<b>Mnemonic</b>	“Microserver”	“Desktop”	“Embedded”
<b>Host Processor</b>	Xilinx Zynq Dual-core ARM A9 XC7Z010		Xilinx Zynq Dual-core ARM A9 XC7Z020
<b>Coprocessor</b>	Epiphany 16-core CPU E16G301		
<b>Memory</b>	1 GB DDR3		
<b>Ethernet</b>	Gigabit Ethernet		
<b>Boot Flash</b>	128Mb QSPI Flash		
<b>Power</b>	5V DC		
<b>Storage</b>	Micro-SD		
<b>USB</b>	No	USB 2.0 Host Port	
<b>HDMI</b>	No	Micro HDMI	
<b>GPIO Pins</b>	0	24	48
<b>eLink Connectors</b>	0	2	2
<b>FPGA Logic</b>	28K Logic Cells 80 DSP Slices	28K Logic Cells 80 DSP Slices	80K Logic Cells 220 DSP slices
<b>Weight</b>	1.3 oz (36 grams)	1.4 oz (38 grams)	
<b>Size</b>	3.5" x 2.1" x 0.625" (90mmx55mmx18mm)		
<b>SKU</b>	P1600-DKxx	P1601-DKxx	P1602-DKxx
<b>HTS Code (Schedule B)</b>	8471.41.0150	8471.41.0150	8471.41.0150

Table 1: Parallella Feature Summary

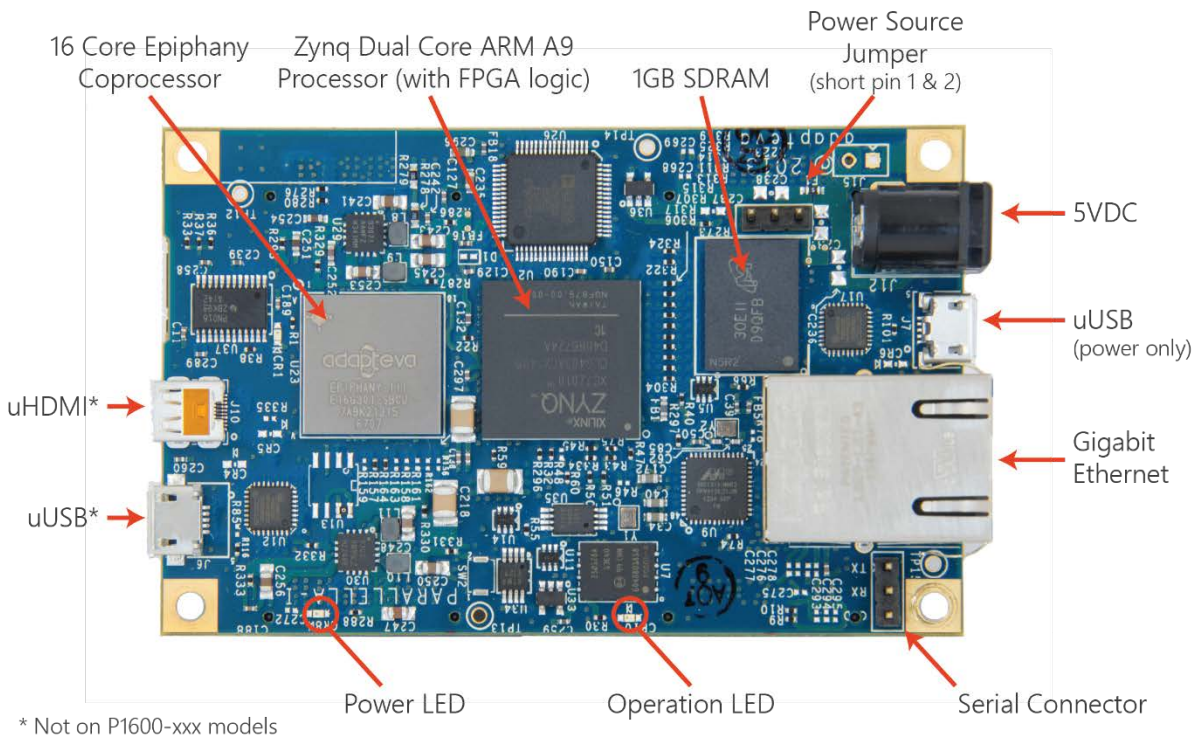


Figure 1: The Parallella Board (top view)

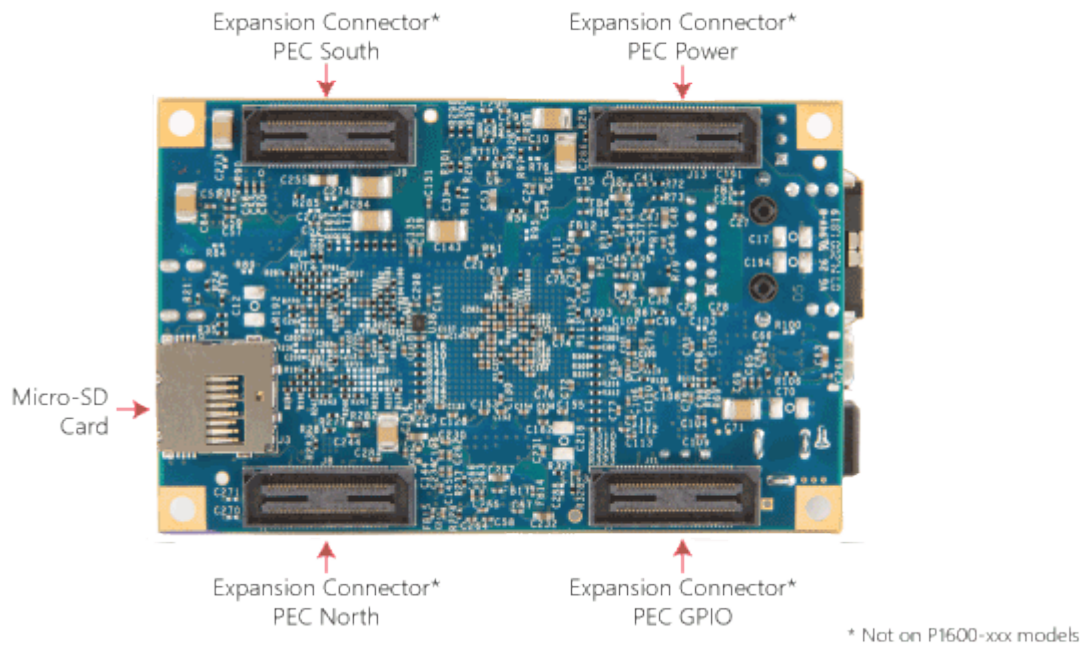


Figure 2: The Parallella Board (bottom view)

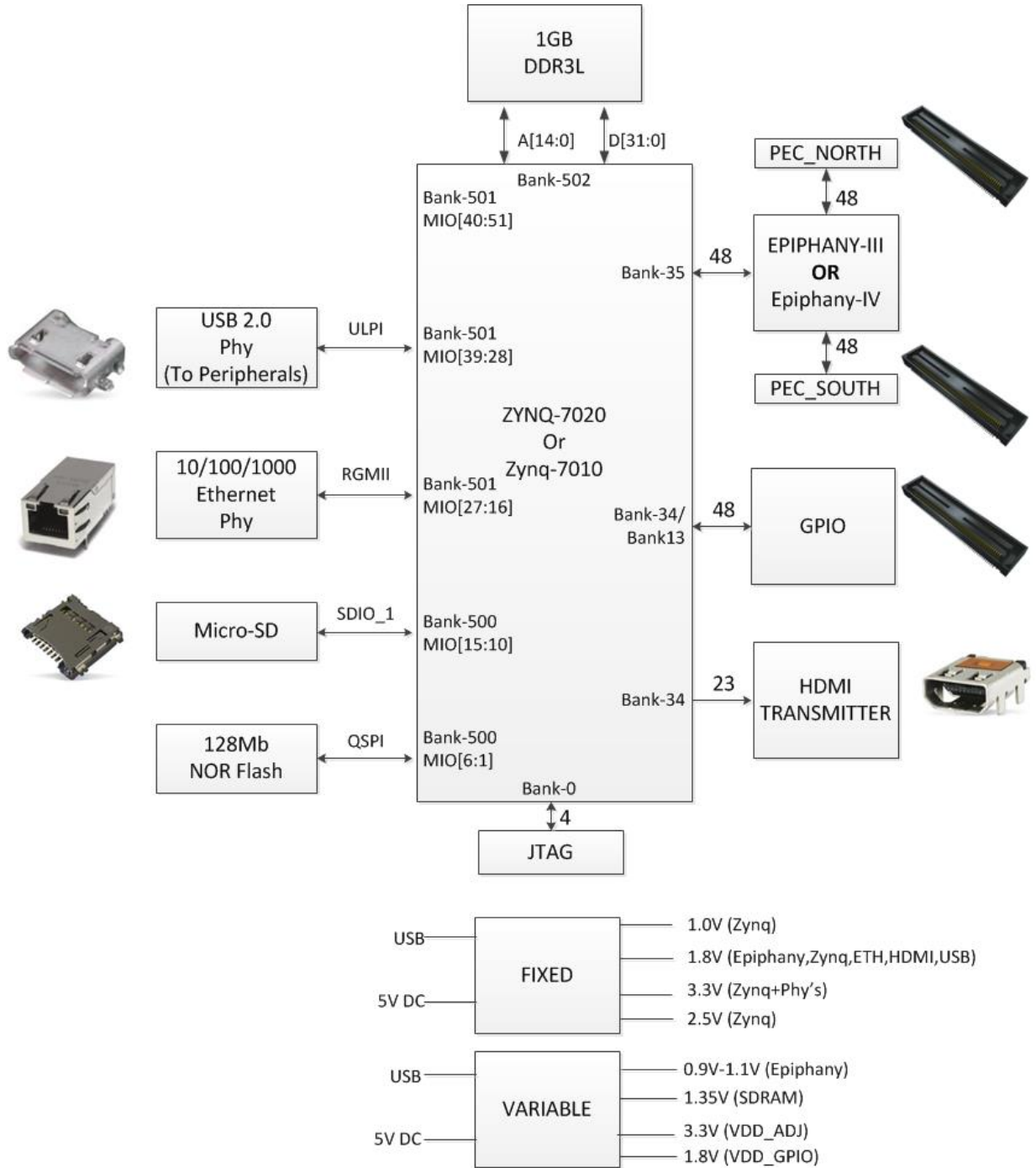


Figure 3: Zynq Connectivity Diagram

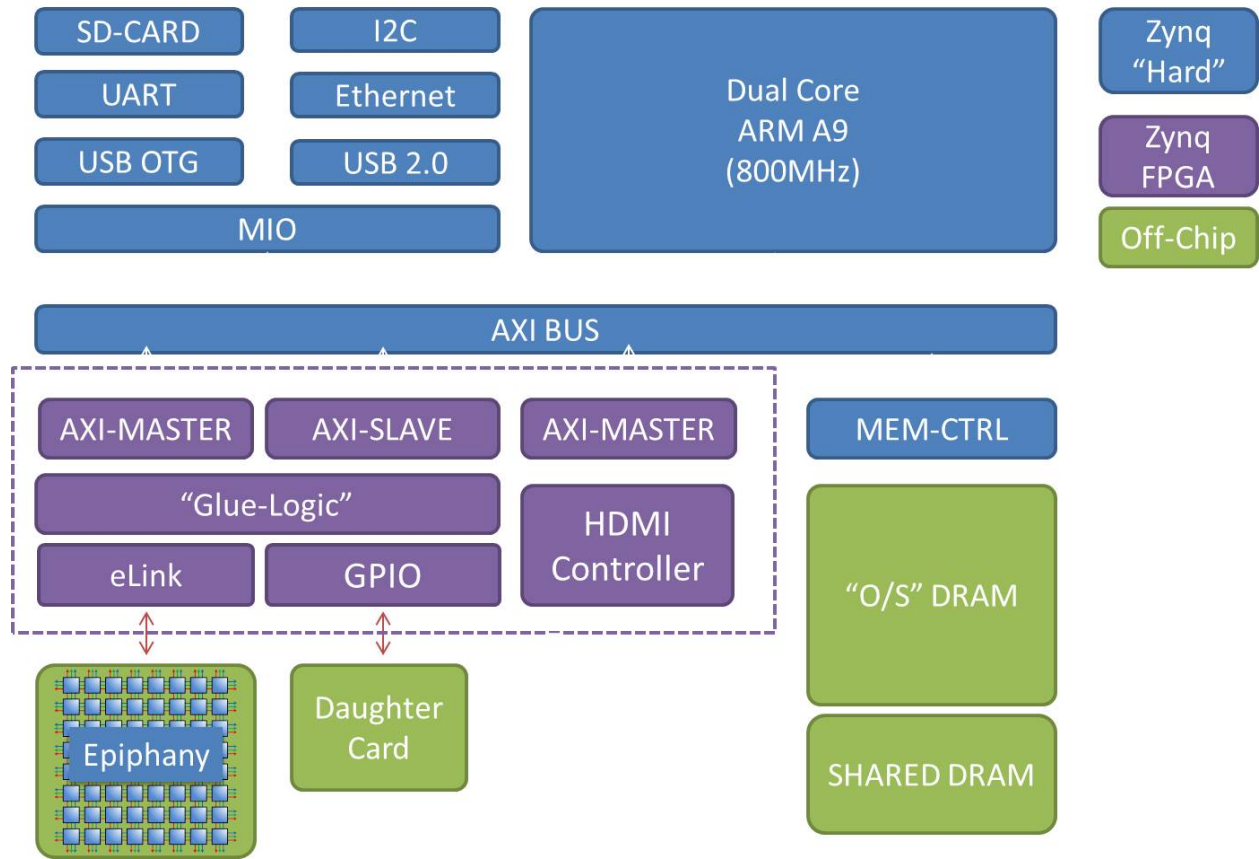
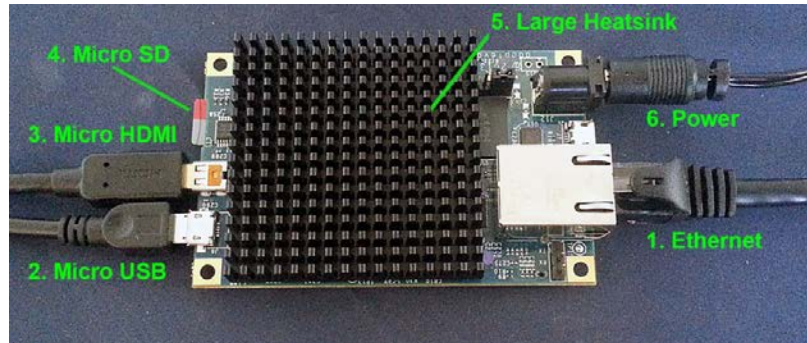


Figure 4: Parallella High Level Architecture

## 2 Quick Start Guide

This section is a summary of the quick start guide is found at [www.parallella.org/quick-start](http://www.parallella.org/quick-start)



### Step 1: Ensure that you have the required accessories

- A high quality 2000mA rated 5V DC power supply with 5.5mm OD / 2.1mm ID center positive polarity plug.
- An ethernet cable
- A fan (required for boards sold before July 10th, 2014, recommended for all others)
- A micro HDMI to HDMI cable (not needed for headless option)
- A USB male Micro-B to female Standard-A cable (not needed for headless option)

### Step 2: Create a bootable micro-SD card

Burn a fresh Micro-SD card using the latest distribution.

- [Instructions for creating an SD card](#)

Note: Burn a fresh SD card even if you were shipped a pre-programmed micro-SD card!

### Step 3: Familiarize yourself with known issues

- The board does get hot so you have to take precautions to cool the board properly. Before letting the board run for hours, you must ensure that the board doesn't overheat. (preferably by using the ['xtemp' utility](#).)
- Boards used without a fan must be placed vertically.
- The Parallella is sensitive to static discharge and must be handled appropriately.
- If you were shipped a board before March 1st, 2014, then you must use a conforming powered USB hub.
- If you were shipped a board before July 10th, 2014 then you must use a fan with the board. (we do still recommend a fan for all customers, especially if you are going to push the performance of the board)

#### **Step 4. Connect peripherals, fit the heat-sink and apply power**

- Connect the cables as indicated by #1-4 in the picture above
- Attach a heatsink to the Zynq device (#5 in right hand picture) OR [install the new large heatsink onto the Parallella board](#)
- Make sure a fan is directed at the board if required. A fan is required when using the small heatsink (right hand picture above). With the large heatsink (left hand picture above) the board will function in normal conditions without requiring a fan, depending on your usage. Monitor the temperature using a utility such as xtemp, and keep the chip temp below 70 degrees Celsius.
- Apply power (#6 in picture)

#### **Step 5: Build and run a program**

The system will boot and a login screen will appear.

Login with the username `linaro` and password `linaro`.

### 3 Feature Descriptions

#### 3.1 Introduction

The Parallella-1.x board uses the components listed in the table below.

Device	Part Number (and datasheet link)
CPU	<a href="#">Zynq™-7000 AP SoC</a>
Epiphany	<a href="#">E16G301</a> and <a href="#">E64G401</a>
Eth PHY	<a href="#">88E1318</a>
USB PHY	<a href="#">USB3320C-EZK-TR</a>
HDMI PHY	<a href="#">ADV7513BSWZ</a>
SDRAM	<a href="#">MT41K256M32SLD</a>
Flash	<a href="#">N25Q128A13EF840E</a>
PMIC #1	<a href="#">ISL9307</a>
PMIC #2	<a href="#">ISL9305</a>

Table 2: Parallella IC summary

#### 3.2 CPU

The central processor on the Parallella board is the [Zynq™-7000 AP SoC](#). The Zynq represents a new class of processor product which combines an industry-standard ARM® dual-core Cortex™-A9 MPCore™ processing system with Xilinx 28nm programmable logic. The Zynq SoC includes the following set of features:

Dual-core ARM® Cortex™-A9 CPU:

- Coherent multiprocessor support
- ARMv7-A architecture
- 32 KB Level 1 4-way set-associative instruction/data caches (independent for each CPU)
- 512 KB 8-way set-associative Level 2 cache shared between CPUs
- TrustZone® security
- Jazelle® RCT execution Environment Architecture
- NEON™ media-processing engine
- Single and double precision Vector Floating Point Unit (VFPU)
- CoreSight™ and Program Trace Macrocell (PTM)
- Three watchdog timers, one global timer, two triple-timer counters

#### I/O Peripherals and Interfaces:

- 10/100/1000 tri-speed Ethernet MAC peripherals GMII, RGMII, and SGMII interfaces
- Two USB 2.0 OTG peripherals
- Two full CAN 2.0B compliant CAN bus interfaces
- Two SD/SDIO 2.0/MMC3.31 compliant controllers
- Two full-duplex SPI ports with three peripheral chip selects
- Two high-speed UARTs (up to 1 Mb/s)
- Two master and slave I2C interfaces
- 8-Channel DMA Controller with scatter/gather capability
- JTAG port for ARM debugging and FPGA programming
- 12 bit ADC input
- On-chip voltage and temperature sensing

#### Programmable Logic:

- LVCMOS, LVDS, and SSTL signaling with 1.2V to 3.3V IO
- Easily accessible from ARM cores through AXI bus(master or slave)
- Up to 125 programmable IO pins (Z-7020)
- Up to 85K programmable logics cells (Z-7020)
- Up to 560 KB distributed RAM (Z-7020)
- Up to 220 DSP slice and (Z-7020)

The Parallella board can be built with two different pin compatible Zynq devices: Zynq Z-7010 or the Zynq Z-7020. The major differences between the Z-7010 and Z-7020 are summarized in Table 4:

	Z-7010	Z-7020
Programmable Logic Cells	28K	85K
Look-Up Tables	17,600	53,200
Flip-flops	35,200	106,400
Extensible Block RAM	240KB	560KB
Programmable DSP Slices	80	220
Bank-13 IO Pins	No	Yes

Table 3: Zynq Feature Summary



### 3.3 Epiphany Coprocessor

The Parallella-16 includes the E16G301 device with 16 CPU cores and the Parallella-64 includes the E64G401 device with 64 CPU cores. Both devices have the following basic features:

Epiphany Core (eCore):

- 32-bit dual-issue superscalar RISC architecture
- Quad-bank 32KB local single cycle access memory
- Floating point instruction set (IEEE754)
- 64-entry register file
- Dual channel DMA engine
- Two 32-bit timers
- Nested interrupt controller
- Memory protection unit
- Debug unit

Network-On-Chip (eMesh):

- Three separate networks:
  - rMesh for read transactions
  - xMesh for off-chip write transactions
  - cMesh for on-chip write transactions
- “API-less” network that processes regular load/store transactions
- All transactions are complete and atomic 104 bit transactions (32 bit address, 64 bit data, and 8 control bits)
- Round robin arbitration at every mesh node
- Mesh network extends off chip enabling glue-less multi-chip design

Chip-To-Chip Links (eLink):

- North, east, west, south links for connecting to other Epiphany chips, FPGAs, or ASICs
- Source synchronous LVDS links with transmit clock aligned in the middle of the data eye
- Dual data rate communication (positive and negative edge transfers)
- Max transfer of 2 bytes transferred in and out simultaneously per link per clock cycle
- Automatic bursting for sequential 64-bit write transactions

### 3.4 SDRAM

1GB 32-bit wide DDR3L SDRAM

### 3.5 Flash

128Mb QSPI Flash Memory for boot code

### 3.6 Gigabit Ethernet

10/100/1000 Ethernet, RJ45 connector with magnetics.

### 3.7 USB 2.0 Host Port

Connects to peripheral devices such as mice, keyboard, camera, etc.

### 3.8 Micro SD

Primary boot source and main Parallella board storage medium.

### 3.9 HDMI Port

A high quality connection to modern DVI/HDMI monitors and TVs through a micro-HDMI connector.

### 3.10 LED Indicators

- A green LED controlled by the Zynq GPIO pin.
- A red LED controlled by the Epiphany flag pin
- Two LEDs on the RJ45. The left LED indicates link speed. (amber=1Gb, green=100Mb, off=10Mb). The right indicates that there is activity on the port.

### 3.11 Serial Port

A three-pin header for 3.3V UART output from the Zynq.

### 3.12 I2C

A 5V I2C interface is available through the PEC\_POWER connector.

### 3.13 Audio

Audio is available through the HDMI connector and through the SPDIF pin on the PEC\_POWER connector.

### 3.14 Analog Input

A differential analog input is available on the PEC\_POWER connector that is sampled by the Zynq built in Analog to Digital Converter.

### 3.15 JTAG Debugging

FPGA programming and debugging of programs running on the Zynq is possible through the JTAG pins on the PEC\_POWER connector.

### 3.16 Powering the board

The Parallella should be powered through a stable 5V/2A power supply. The following methods are available for connecting a 5V supply. Current consumption for the Parallella board can be as low as 0.3A but can reach 1.5A when fully loaded.

Recommended Methods (choose one only):

- **J12:** 5.5mm OD / 2.1mm ID center positive barrel connector (place jumper on J14 in 1-2 position)
- **J7:** micro-USB connector (place jumper on J14 in 2-3 position)

Experimental (at your own risk):

- **PTH1:** Mounting hole. Need to install/solder and short J15
- **J13:** Pins 1 and 2 of the PEC\_POWER connector

### 3.17 Parallella On-Board Power Management

The on-board power rails are regulated by the Intersil PMICs ISL9307 and ISL9305 as shown in the following Figure.

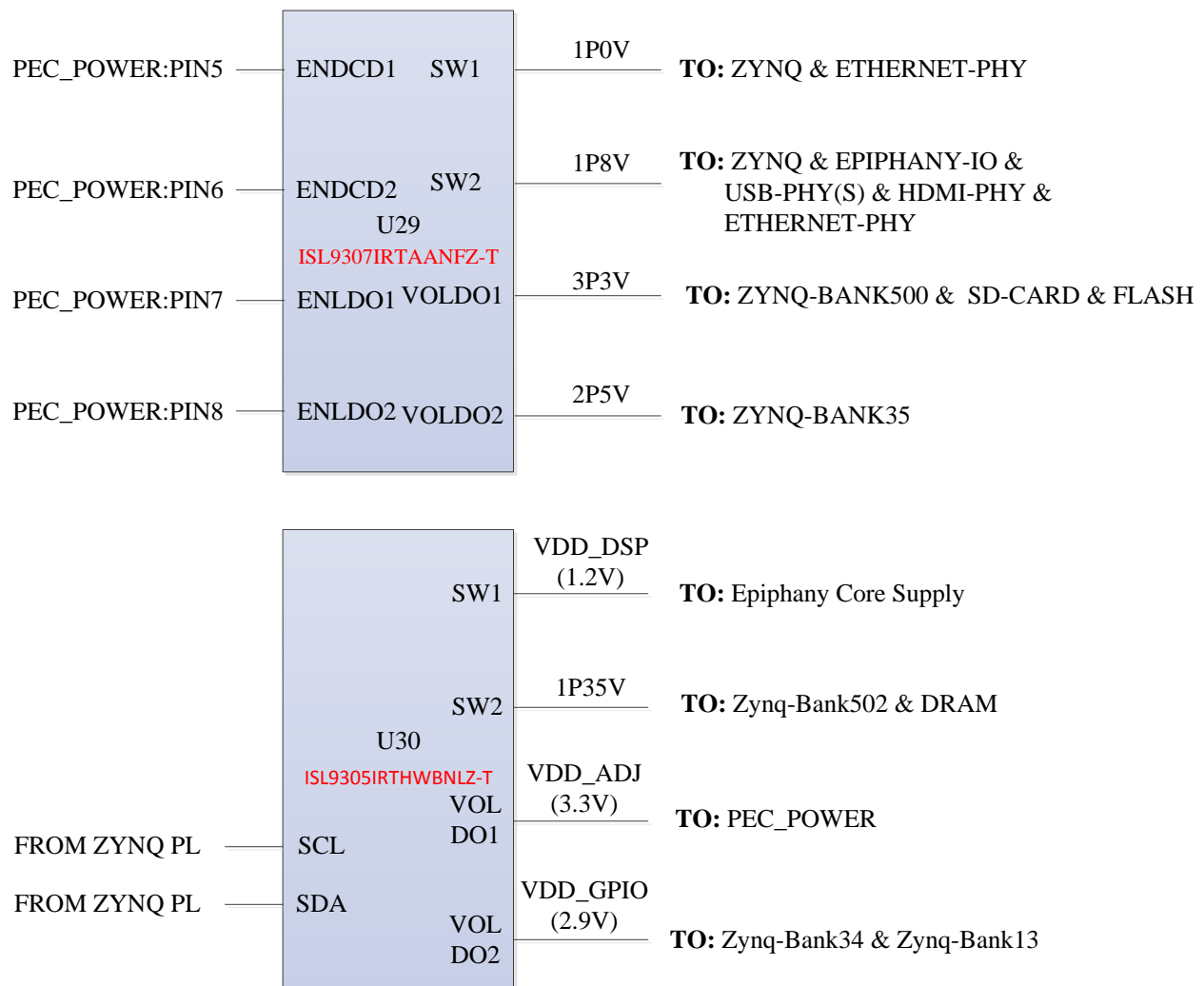


Figure 5: Power Management

All four voltage rail outputs on the ISL9305 can be set by programming the appropriate registers within the chip using the I2C interface. The Parallella on-board flash contains the appropriate programming sequence to set the VDD\_DSP rail to 1.0V and the VDD\_GPIO rail to 2.5V automatically at boot time.

### 3.18 Parallella Supply Outputs

The Parallella can power expansion/daughter cards directly using the PEC\_POWER connector.

The following voltages are available at the PEC\_POWER connector:

- 5V
- 3.3V
- 2.5V
- VADJ
- VAD\_GPIO
- 1.8V
- 1.35V
- 1.0V (Zynq)
- 1.0V (Epiphany)

The two on-board PMICs can deliver 1.5A on each step-down converter output and 300mA on each general purpose LDO output. The amount of current drawn by the Parallella board will depend on the level of activity on the board and the amount of current left over for the expansion card is yet to be characterized.

NOTE: At this time, the PEC\_POWER feature should be considered experimental. The safest power solution for expansion cards is to: 1.) Have a completely independent power sub system or 2.) To use the 5V PEC\_POWER rail.

Each one of the Parallella rails can also be powered directly from the PEC\_POWER connector instead of from the on board power management ICs. Each rail to be driven from an external connector would first need to be powered down appropriately to avoid damaging the circuitry. To disable one of the ISL7307 outputs, pull down the corresponding REG\_EN\* signal available on the PEC\_POWER connector. To disable one of the ISL9305 outputs, program the appropriate registers using the I2C interface.

NOTE: There WILL be permanent damage to the board the power rails are driven incorrectly. Please exercise extreme caution!

### 3.19 Parallella Expansion Connectors

The Parallella board has four expansions connectors placed on the opposite edges of the bottom side of the board shown in Figure 2. For exact connector and placement information, please refer to the Parallella mechanical drawings. The following figure shows the expansion connector placements as seen from the bottom side of the board.

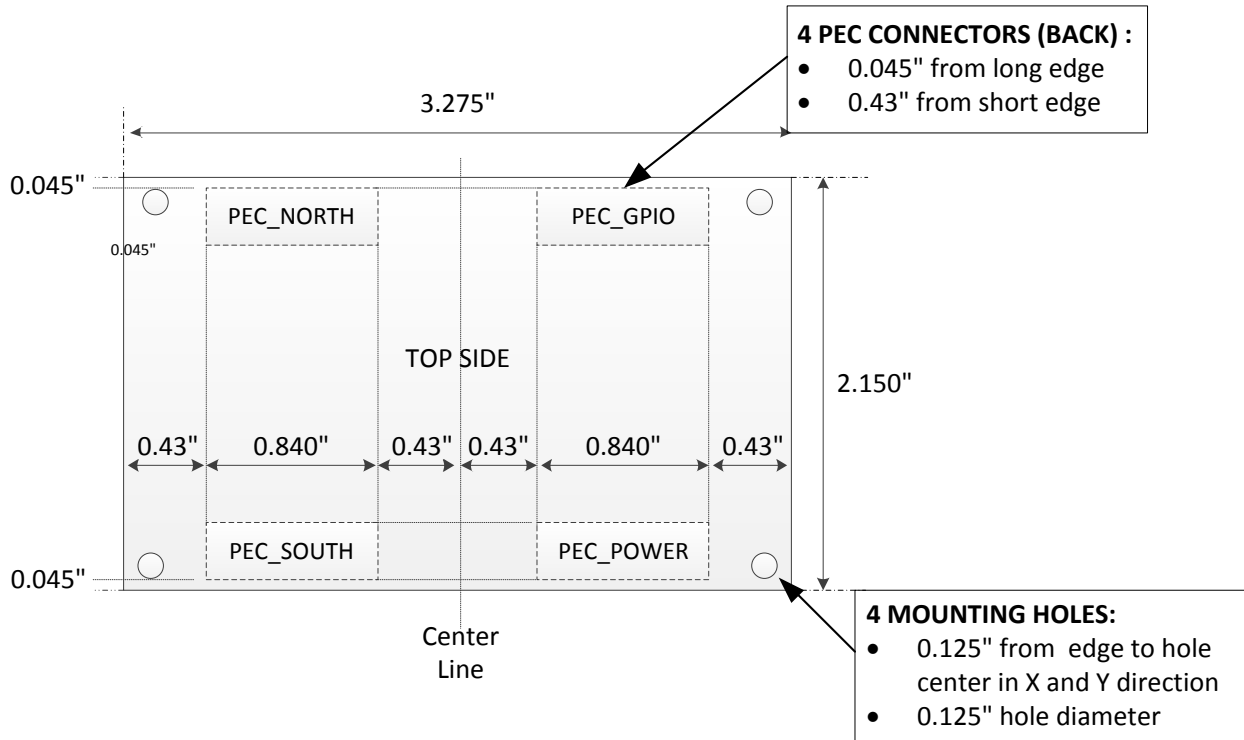


Figure 6: PEC Placement Diagram

The Parallella Expansion Connectors uses the 60 pin BSH-030-01-FDA high speed connector from Samtec. The corresponding mating connector to be placed on the expansion card is BTH-030-01-FDA. The complete data sheets can be found at:

<https://www.samtec.com/technical-specifications/Default.aspx?SeriesMaster=BSH>

A complete characterization report for the Samtec connectors can be found at:

[http://www.samtec.com/Documents/WebFiles/TestRpt/172630\\_report\\_rev\\_2\\_qua.pdf](http://www.samtec.com/Documents/WebFiles/TestRpt/172630_report_rev_2_qua.pdf)

Connector	Functions
PEC_POWER	Power and control signal expansion connector
PEC_FPGA	Zynq programmable logic expansion connector
PEC_NORTH	Epiphany north link expansion connector
PEC_SOUTH	Epiphany south link expansion connector

Figure 7: Parallella Expansion Connectors (PEC)

The four symmetrically placed connectors allow for robust mating of expansion cards and the Parallella board using matching BTH-030-01-FDA connectors. As shown in Figure 5, it is possible to connect a single full length credit card sized expansion cards or two half-length expansion cards. The left side shows two half-length expansion boards (pink/green transparent) connected to the backside of the Parallella board

and the right side shows a full length (blue transparent) expansion board connected to the backside of the Parallella board.

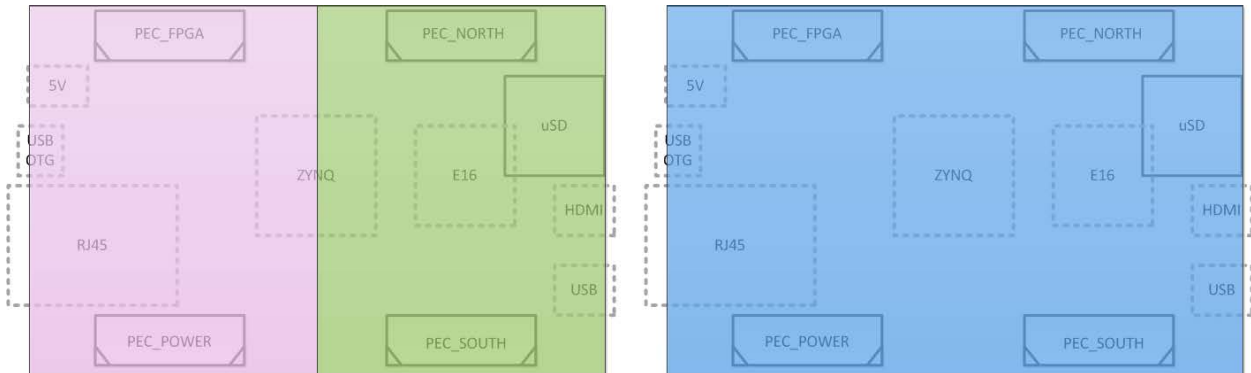


Figure 8: Daughter Card Configurations

### 3.20 Mounting Holes

The board has four symmetrically placed mounting holes, one in each corner. The mounting holes have a diameter of 0.125”.

Three of the mounting holes are connected to ground while the fourth mounting hole is floating by default. This floating mounting hole can be connected to the 5V supply as a build or solder option, allowing power to be easily applied to a stack of Parallella boards without the need for extensive 5V DC cabling.

## 4 Parallella System Architecture

### 4.1 Zynq Memory Map

The following Table shows the hard-coded memory architecture of the Zynq architecture most relevant to the Parallella architecture. For a complete description of the Zynq of the memory architecture, please refer to the Architecture Reference manual for the Zynq.

Address Start	Address End	Size	Function	Note
0x0010_0000	0x3FFF_FFFF	1GB	DRAM	Accessible to all interconnect masters
0x4000_0000	0x7FFF_FFFF	1GB	PL	Custom logic address range
0x8000_0000	0xBFFF_FFFF	1GB	PL	Epiphany address range
0xFC00_0000	0xFCFF_FFFF	16MB	FLASH	Quad-SPI linear address for linear mode
0xFFFC_0000	0xFFFF_FFFF	252KB	OCM	OCM upper address range

Figure 9: Zynq Memory Map

The ARM communicates with programmable logic, GPIO connected to the programmable logic, and the Epiphany by accessing the memory ranges shown in the table.

The Epiphany 32-bit memory space is mapped into the Zynq memory space allowing for easy sharing of data and resources between the ARM and the Epiphany. The Epiphany address range is a matter of convention and depends on the appropriate AXI master and slave interfaces being implemented within the programmable logic on the Zynq.

## 4.2 Epiphany Memory Map

The Epiphany chip is situated within a 1GB section within the Zynq host processor memory map. The offset within the 1GB space occupied by an Epiphany coprocessor is set by the ROWID and COLID pins on the Epiphany chip. The ROWID and COLID can be individually set on boards through the PEC\_POWER connector enabling direct board to board connection through the PEC\_NORTH and PEC\_SOUTH connectors. By default the address locations of the Epiphany cores on Parallella-16 are as shown in the Table below.

Core Number	Start Address	End Address	Size
(32,8)	80800000	80807FFF	32KB
(32,9)	80900000	80907FFF	32KB
(32,10)	80A00000	80A07FFF	32KB
(32,11)	80B00000	80B07FFF	32KB
(33,8)	84800000	84807FFF	32KB
(33,9)	84900000	84907FFF	32KB
(33,10)	84A00000	84A07FFF	32KB
(33,11)	84B00000	84B07FFF	32KB
(34,8)	88800000	88807FFF	32KB
(34,9)	88900000	88907FFF	32KB
(34,10)	88A00000	88A07FFF	32KB
(34,11)	88B00000	88B07FFF	32KB
(35,8)	8C800000	8C807FFF	32KB
(35,9)	8C900000	8C907FFF	32KB
(35,10)	8CA00000	8CA07FFF	32KB
(35,11)	8CB00000	9CB07FFF	32KB

Figure 10: Epiphany Memory Map



### 4.3 Epiphany Specific FPGA Resources

Developers that want leverage the Epiphany co-processors should use the Parallella programmable logic reference design with minimal changes for best results. The following registers must be accessible by the Epiphany drivers from the ARM for correct operation.

Register	Address	Bits	Details
ESYSCONFIG	0x808f0f00	[0]	Enable transaction timeout on read from Zynq
		[2:1]	00: Filter disable 01: Inclusive range. Block transactions inside REG_FILTERL and REG_FILTERH range) 10: Exclusive range. Block transactions outside REG_FILTERL and REG_FILTERH range) 11: Reserved
		[3]	Epiphany eLink enable 0:→ 1.) Forces RESET_N to zero, 2.) turns off the epiphany input clock cclk 3.) and turns off the elink TX/RX in the FPGA 1:→ 1.) Turns on epiphany clock, 2.) forces RESET_N to one (“out of reset”) 3.) Turns on elink RX/TX in the FPGA
		[27:4]	Reserved
		[31:28]	Epiphany transaction control mode
ESYSRESET	0x808f0f04		A write transaction to this register asserts a reset signal to Epiphany and the eLink logic within the Zynq.

ESYSINFO	0x808f0f08	[7:0]	Platform #: 0=undefined 1=parallella-1.x,e16,7z020,gpio 2=parallella-1.x,e16,7z020,no-gpio 3=parallella-1.x,e16,7z010,gpio 4=parallella-1.x,e16,7z010,no-gpio 5=parallella-1.x,e64,7x020,gpio
		[15:8]	FPGA load type #: 0=undefined 1=hdmi enabled, gpio unused 2=headless, gpio unused
		[23:16]	Revision #: 0=undefined 1=first version 2=second version 3=etc..
ESYSFILTERL	0x808f0f0c	[31:0]	32-bit Transaction Filter (Low), [1:0] are ignored
ESYSFILTERH	0x808f0f10	[31:0]	32-bit Transaction Filter (High), [1:0] are ignored
ESYSFILTERC	0x808f0f14	[31:2]	Captured address of a filter violation
		[1:0]	Filter capture status 00 - not a valid value 01 - First violating transaction 10 - Second violating transaction 11 - There are more than 3 violating transactions A write to this register clears value to zero

**Table 4: Epiphany System Registers**

The Epiphany coprocessor is connected to the Zynq SOC via the 48-pin eLink interface. An Epiphany eLink protocol is implemented in the programmable logic portion of the Zynq SOC. In addition to the eLink interface, the programmable logic within the Parallella board includes an AXI master interface, an AXI slave interface, and an optional HDMI controller interface.

## 5 Board Configuration

### 5.1 FPGA Pin Assignment

The following table shows the pin assignment of the programmable logic within the Zynq FPGA. A text version of this table “UCF file”, can be found at:

Net Name	Zynq Pin	Direction	IOSTANDARD
HDMI_D8	Y18	output	LVCNMOS25
HDMI_D9	W18	output	LVCNMOS25
HDMI_D10	V18	output	LVCNMOS25
HDMI_D11	V15	output	LVCNMOS25
HDMI_D12	R18	output	LVCNMOS25
HDMI_D13	P18	output	LVCNMOS25
HDMI_D14	Y19	output	LVCNMOS25
HDMI_D15	W19	output	LVCNMOS25
HDMI_D16	W15	output	LVCNMOS25
HDMI_D17	T19	output	LVCNMOS25
HDMI_D18	R19	output	LVCNMOS25
HDMI_D19	P19	output	LVCNMOS25
HDMI_D20	W20	output	LVCNMOS25
HDMI_D21	V20	output	LVCNMOS25
HDMI_D22	U20	output	LVCNMOS25
HDMI_D23	T20	output	LVCNMOS25
HDMI_CLK	R17	output	LVCNMOS25
HDMI_VSYNC	V17	output	LVCNMOS25
HDMI_HSYNC	T17	output	LVCNMOS25
HDMI_DE	Y17	output	LVCNMOS25
SPDIF	Y16	output	LVCNMOS25
HDMI_INT	P20	input	LVCNMOS25
PS_I2C_SCL	N18	inout	LVCNMOS25

PS_I2C_SDA	N17	inout	LVCMOS25
PROG_IO	N20	inout	LVCMOS25
TURBO_MODE	R16	input	LVCMOS25
GPIO0_P	T16	inout	LVDS_25
GPIO0_N	U17	inout	LVDS_25
GPIO1_P	V16	inout	LVDS_25
GPIO1_N	W16	inout	LVDS_25
GPIO2_P	P15	inout	LVDS_25
GPIO2_N	P16	inout	LVDS_25
GPIO3_P	U18	inout	LVDS_25
GPIO3_N	U19	inout	LVDS_25
GPIO4_P	P14	inout	LVDS_25
GPIO4_N	R14	inout	LVDS_25
GPIO5_P	T14	inout	LVDS_25
GPIO5_N	T15	inout	LVDS_25
GPIO6_P	U14	inout	LVDS_25
GPIO6_N	U15	inout	LVDS_25
GPIO7_P	W14	inout	LVDS_25
GPIO7_N	Y14	inout	LVDS_25
GPIO8_P	U13	inout	LVDS_25
GPIO8_N	V13	inout	LVDS_25
GPIO9_P	V12	inout	LVDS_25
GPIO9_N	W13	inout	LVDS_25
GPIO10_P	T12	inout	LVDS_25
GPIO10_N	U12	inout	LVDS_25
GPIO11_P	T11	inout	LVDS_25
GPIO11_N	T10	inout	LVDS_25

**Table 5: Zynq Bank32 Pin Assignments**

Net Name	Zynq Pin	Direction	IOSTANDARD
RXI_CCLK_P	H16	output	LVDS_25
RXI_CCLK_N	H17	output	LVDS_25
DSP_RESET_N	G14	output	LVCMOS25
RXI_LCLK_P	F16	output	LVDS_25
RXI_LCLK_N	F17	output	LVDS_25
RXI_DATA0_P	B19	output	LVDS_25
RXI_DATA0_N	A20	output	LVDS_25
RXI_DATA1_P	C20	output	LVDS_25
RXI_DATA1_N	B20	output	LVDS_25
RXI_DATA2_P	D19	output	LVDS_25
RXI_DATA2_N	D20	output	LVDS_25
RXI_DATA3_P	E18	output	LVDS_25
RXI_DATA3_N	E19	output	LVDS_25
RXI_DATA4_P	E17	output	LVDS_25
RXI_DATA4_N	D18	output	LVDS_25
RXI_DATA5_P	F19	output	LVDS_25
RXI_DATA5_N	F20	output	LVDS_25
RXI_DATA6_P	G17	output	LVDS_25
RXI_DATA6_N	G18	output	LVDS_25
RXI_DATA7_P	G19	output	LVDS_25
RXI_DATA7_N	G20	output	LVDS_25
RXI_FRAME_P	H15	output	LVDS_25
RXI_FRAME_N	G15	output	LVDS_25
RXO_RD_WAIT	J15	input	LVCMOS25
RXO_RD_WAIT_P	J18	input	LVCMOS25
RXO_WR_WAIT_N	H18	input	LVDS_25
TXO_LCLK_P	K17	input	LVDS_25
TXO_LCLK_N	K18	input	LVDS_25

TXO_DATA0_P	K19	input	LVDS_25
TXO_DATA0_N	J19	input	LVDS_25
TXO_DATA1_P	L14	input	LVDS_25
TXO_DATA1_N	L15	input	LVDS_25
TXO_DATA2_P	L16	input	LVDS_25
TXO_DATA2_N	L17	input	LVDS_25
TXO_DATA3_P	M14	input	LVDS_25
TXO_DATA3_N	M15	input	LVDS_25
TXO_DATA4_P	L19	input	LVDS_25
TXO_DATA4_N	L20	input	LVDS_25
TXO_DATA5_P	M19	input	LVDS_25
TXO_DATA5_N	M20	input	LVDS_25
TXO_DATA6_P	M17	input	LVDS_25
TXO_DATA6_N	M18	input	LVDS_25
TXO_DATA7_P	N15	input	LVDS_25
TXO_DATA7_N	N16	input	LVDS_25
TXO_FRAME_P	J20	input	LVDS_25
TXO_FRAME_N	H20	input	LVDS_25
TXI_RD_WAIT_N	K14	output	LVDS_25
TXI_RD_WAIT_P	J14	output	LVDS_25
TXI_WR_WAIT_P	K16	output	LVDS_25
TXI_WR_WAIT_N	J16	output	LVDS_25

**Table 6: Zynq Bank 34 Pin Assignments**

Net Name	Zynq Pin	Direction	IOSTANDARD
GPIO12_P	Y12	inout	LVDS_25
GPIO12_N	Y13	inout	LVDS_25
GPIO13_P	W11	inout	LVDS_25
GPIO13_N	Y11	inout	LVDS_25
GPIO14_P	V11	inout	LVDS_25
GPIO14_N	V10	inout	LVDS_25
GPIO15_P	T9	inout	LVDS_25
GPIO15_N	U10	inout	LVDS_25
GPIO16_P	W10	inout	LVDS_25
GPIO16_N	W9	inout	LVDS_25
GPIO17_P	U9	inout	LVDS_25
GPIO17_N	U8	inout	LVDS_25
GPIO18_P	W8	inout	LVDS_25
GPIO18_N	Y9	inout	LVDS_25
GPIO19_P	Y8	inout	LVDS_25
GPIO19_N	Y7	inout	LVDS_25
GPIO20_P	Y6	inout	LVDS_25
GPIO20_N	U7	inout	LVDS_25
GPIO21_P	V7	inout	LVDS_25
GPIO21_N	V6	inout	LVDS_25
GPIO22_P	W6	inout	LVDS_25
GPIO22_N	T5	inout	LVDS_25
GPIO23_P	U5	inout	LVDS_25

**Table 7: Zynq Bank 13 Pin Assignments**

## 6 Booting the Parallella



## 7 Parallella Expansion Connector Details

### 7.1 PEC\_POWER

The PEC\_POWER provides convenient access to various key Parallella board signals and can provide power to expansion boards with modest current requirements. Expansion boards with substantial current requirements should draw power from the SYS\_5P0V connection or generate supply rails from a completely independent DC supply.

Signal	Direction	Max	Notes
SYS_5P0V	Inout	5.0V	Parallella expansion board supply. Driven by output of power selector 3-pin header that selects between DC power and USB power.
1P0V	Inout	1.0V	Core voltage for Zynq and Ethernet PHY. Driven by 1.5A switching regulator output of PMIC.
VDD_DSP	Inout	1.0V	Core voltage for Epiphany coprocessor. Driven by 1.5A switching regulator output of PMIC.
1P35V	Inout	1.35V	Supply shared by Zynq and DDR3L SDRAM. Driven by 1.5A switching regulator output of PMIC.
1P8V	Inout	1.8V	General purpose voltage shared by USB PHY, Ethernet PHY, Epiphany, Zynq, and HDMI. Driven by 1.5A switching regulator output of PMIC.
2P5V	Inout	2.5V	IO voltage for Zynq LVDS interface that communicates with the Epiphany coprocessor. Driven by 300mA LDO output of PMIC.
3.3V	Inout	3.3V	IO voltage for Zynq, HDMI, and flash chip. Driven by 300mA LDO output of PMIC.
VDD_GPIO	Inout	3.3V	IO voltage for Zynq, HDMI, and flash chip. Driven by 300mA LDO output of PMIC.
VDD_ADJ	Inout	3.3V	Independent supply output for expansion cards. Driven by 300mA LDO output on PMIC.
GND	Inout	0.0V	System Ground
I2C_SDA	Inout	5.0V	I2C bidirectional open-drain Serial Data Line
I2C_SCL	Inout	5.0V	I2C bidirectional open-drain Serial Clock Line
UART_TX	Output	3.3V	UART transmit signal
UART_RX	Input	3.3V	UART receive signal

SPDIF	Output	2.5V	Single bit SPDIF audio interface output
RESET_N	Output	3.3V	Active low Parallella board reset signal
USER_LED	Output	3.3V	On board LED signal driven by Zynq
DSP_XID[3:0]	Input	1.8V	Sets the relative chip column ID of the Epiphany chip on the Parallella board, overriding the default board settings. These signals must be driven correctly in systems that utilize the PEC_NORTH/PEC_SOUTH to connect multiple Parallella boards.
DSP_YID[3:0]	Input	1.8V	Sets the relative chip row ID of the Epiphany chip on the Parallella board, overriding the default board settings. These signals must be driven correctly in systems that utilize the PEC_NORTH/PEC_SOUTH to connect multiple Parallella boards.
DSP_FLAG	Output	1.8V	Flag signal driven by the Epiphany.
TURBO_MODE	Output	3.3V	Not supported
JTAG_BOOT	Input	3.3V	Pull down to zero for JTAG boot
JTAG_TCK	Input	3.3V	JTAG Clock
JTAG_TMS	Input	3.3V	JTAG Test Mode
JTAG_TDI	Input	3.3V	JTAG Data Input
JTAG_TDO	Output	3.3V	JTAG Data Output
REG_EN1	Input	5V	Drive low to disable on-board 1V regulator output
REG_EN2	Input	5V	Drive low to disable on-board 1.8V regulator output
REG_EN3	Input	5V	Drive low to disable on-board 3.3V regulator output
REG_EN4	Input	5V	Drive low to disable on-board 2.5V regulator output

**Table 8: PEC\_POWER Signal Summary**

Signal	Pin	Pin	Signal
SYS_5P0V	1	2	SYS_5P0V
I2C_SCL	3	4	I2C_SDA
REG_EN1	5	6	REG_EN2
REG_EN3	7	8	REG_EN3
PROG_IO	9	10	NC
GND	11	12	GND
DSP_XID[0]	13	14	DSP_YID[0]
DSP_XID[1]	15	16	DSP_YID[1]
DSP_XID[2]	17	18	DSP_YID[2]
DSP_XID[3]	19	20	DSP_YID[3]
GND	21	22	GND
DSP_FLAG	23	24	UART_RX
TURBO_MODE	25	26	UART_TX
SPDIF	27	28	USER_LED
JTAG_BOOT_EN	29	30	RESET_N
GND	31	32	GND
VADC_N	33	34	VADC_P
GND	35	36	GND
JTAG_TMS	37	38	JTAG_TDI
TAG_TCK	39	40	JTAG_TDO
GND	41	42	GND
1P0V	43	44	1P0V
VDD_DSP	45	46	VDD_DSP
1P35V	47	48	1P35V
1P8V	49	50	1P8V
GND	51	52	GND
VDD_ADJ	53	54	VDD_ADJ
VDD_GPIO	55	56	VDD_GPIO
2P5V	57	58	2P5V
3P3V	59	60	3P3V

**Table 9: PEC\_POWER Pin Mapping**

## 7.2 PEC\_FPGA

The PEC\_FPGA can be used to connect the Zynq programmable logic to expansion cards or other PEC\_FPGA interfaces on another Parallella boards. The PEC\_FPGA includes 48 bidirectional signals that can be configured within the Zynq device to support a number of different signal standards, including LVCMOS and LVDS.

Signal	Direction	Notes
VDD_GPIO	Output	Supply driven by power management IC on the Parallella board. Nominal voltage is 2.5V. The PMIC output voltage can be reprogrammed in software through I2C from the Zynq.
GND	Inout	System Ground
GPIOx_{N,P}	Inout	A differential pair or two single ended signals that connect between an expansion card and the Zynq device on the Parallella board.

**Table 10: PEC\_FPGA Signal Summary**

Signal	Pin	Pin	Signal
VDD_GPIO	1	2	VDD_GPIO
GPIO0_N	3	4	GPIO1_N
GPIO0_P	5	6	GPIO1_P
GPIO2_N	7	8	GPIO3_N
GPIO2_P	9	10	GPIO3_P
GND	11	12	GND
GPIO4_N	13	14	GPIO5_N
GPIO4_P	15	16	GPIO5_P
GPIO6_N	17	18	GPIO7_N
GPIO6_P	19	20	GPIO7_P
GND	21	22	GND
GPIO8_N	23	24	GPIO9_N
GPIO8_P	25	26	GPIO9_P
GPIO10_N	27	28	GPIO11_N
GPIO10_P	29	30	GPIO11_P
GND	31	32	GND
GPIO12_N	33	34	GPIO13_N
GPIO12_P	35	36	GPIO13_P
GPIO14_N	37	38	GPIO15_N
GPIO14_P	39	40	GPIO15_P
GND	41	42	GND
GPIO16_N	43	44	GPIO17_N
GPIO16_P	45	46	GPIO17_P
GPIO18_N	47	48	GPIO19_N
GPIO18_P	49	50	GPIO19_P
GND	51	52	GND
GPIO20_N	53	54	GPIO21_N
GPIO20_P	55	56	GPIO21_P
GPIO22_N	57	58	GPIO23_N
GPIO22_P	59	60	GPIO23_P

**Table 11: PEC\_FPGA Pin Mapping**

### 7.3 PEC\_NORTH/PEC\_SOUTH

The PEC\_NORTH and PEC\_SOUTH are connected to the north and south link of the Epiphany chip on the Parallella board. These expansion connectors can be used to connect multiple Parallella boards in a bidirectional line or ring configuration or they can be connected to an FPGA device that has Epiphany eLink interface instantiated inside.

Signal Name	Direction	Signal Description
1P8V	Output	1.8V supply driven by power management IC on the Parallella board.
GND	Inout	System ground
RXI_{NO,SO}_DATA_{P,N}[7:0]	Input	Receiver data
RXI_{NO,SO}_FRAME_{P,N}	Input	Receiver packet framing signal
RXI_{NO,SO}_LCLK_{P,N}	Input	Receiver clock
RXO_{NO,SO}_WR_WAIT_{P,N}	Output	Push-back for transmitter indicating that device must hold off on sending another write packet.
RXO_{NO,SO}_RD_WAIT_{P,N}	Output	Push-back for transmitter indicating that device must hold off on sending another read packet.
TXO_{NO,SO}_DATA_{P,N}[7:0]	Output	Transmitter data
TXO_{NO,SO}_FRAME_{P,N}	Output	Transmitter packet framing signal
TXO_{NO,SO}_LCLK_{P,N}	Output	Transmitter clock
TXI_{NO,SO}_WR_WAIT_{P,N}	Input	Push-back from receiver indicating that transmitter must hold off on sending another write packet.
TXI_{NO,SO}_RD_WAIT_{P,N}	Input	Push-back from transmitter indicating that transmitter must hold off on sending another read packet.

**Table 12: PEC\_NORTH/SOUTH Signal Summary**

Signal	Pin	Pin	Signal
1P8V	1	2	1P8V
RXI NO DATA N[0]	3	4	RXI NO DATA N[1]
RXI NO DATA P[0]	5	6	RXI NO DATA P[1]
RXI NO DATA N[2]	7	8	RXI NO DATA N[3]
RXI NO DATA P[2]	9	10	RXI NO DATA P[3]
GND	11	12	GND
RXI NO DATA N[4]	13	14	RXI NO DATA N[5]
RXI NO DATA P[4]	15	16	RXI NO DATA P[5]
RXI NO DATA N[6]	17	18	RXI NO DATA N[7]
RXI NO DATA P[6]	19	20	RXI NO DATA P[7]
GND	21	22	GND
RXI NO LCLK N	23	24	RXI NO FRAME N
RXI NO LCLK P	25	26	RXI NO FRAME P
RXO NO RD WAIT N	27	28	RXO SO WR WAIT N
RXO NO RD WAIT P	29	30	RXO NO WR WAIT P
GND	31	32	GND
TXO NO FRAME N	33	34	TXI NO WR WAIT N
TXO NO FRAME P	35	36	TXI NO WR WAIT P
TXO NO LCLK N	37	38	TXI NO RD WAIT N
TXO NO LCLK P	39	40	TXI NO RD WAIT P
GND	41	42	GND
TXO NO DATA N[0]	43	44	TXO NO DATA N[1]
TXO NO DATA P[0]	45	46	TXO NO DATA P[1]
TXO NO DATA N[2]	47	48	TXO NO DATA N[3]
TXO NO DATA P[2]	49	50	TXO NO DATA P[3]
GND	51	52	GND
TXO NO DATA N[4]	53	54	TXO NO DATA N[5]
TXO NO DATA P[4]	55	56	TXO NO DATA P[5]
TXO NO DATA N[6]	57	58	TXO NO DATA N[7]
TXO NO DATA P[6]	59	60	TXO NO DATA P[7]

**Table 13: PEC\_NORTH Pin Mapping for Parallella-16**

Signal	Pin	Pin	Signal
1P8V	1	2	1P8V
TXO NO DATA P[7]	3	4	TXO NO DATA P[6]
TXO NO DATA N[7]	5	6	TXO NO DATA N[6]
TXO NO DATA P[5]	7	8	TXO NO DATA P[4]
TXO NO DATA N[5]	9	10	TXO NO DATA N[4]
GND	11	12	GND
TXO NO DATA P[3]	13	14	TXO NO DATA P[2]
TXO NO DATA N[3]	15	16	TXO NO DATA N[2]
TXO NO DATA P[1]	17	18	TXO NO DATA P[0]
TXO NO DATA N[1]	19	20	TXO NO DATA N[0]
GND	21	22	GND
TXO NO LCLK P	23	24	TXI NO RD WAIT P
TXO NO LCLK N	25	26	TXI NO RD WAIT N
RXO NO WR WAIT P	27	28	RXO NO RD WAIT P
RXO NO WR WAIT N	29	30	RXO NO RD WAIT N
GND	31	32	GND
TXO NO FRAME P	33	34	TXI NO WR WAIT N
TXO NO FRAME N	35	36	TXI NO WR WAIT P
RXI NO LCLK P	37	38	RXI NO FRAME P
RXI NO LCLK N	39	40	RXI NO FRAME N
GND	41	42	GND
RXI NO DATA P[7]	43	44	RXI NO DATA P[6]
RXI NO DATA N[7]	45	46	RXI NO DATA N[6]
RXI NO DATA P[5]	47	48	RXI NO DATA P[4]
RXI NO DATA N[5]	49	50	RXI NO DATA N[4]
GND	51	52	GND
RXI NO DATA P[3]	53	54	RXI NO DATA P[2]
RXI NO DATA N[3]	55	56	RXI NO DATA N[2]
RXI NO DATA P[1]	57	58	RXI NO DATA P[0]
RXI NO DATA N[1]	59	60	RXI NO DATA N[0]

**Table 14: PEC\_NORTH Pin Mapping for Parallella-64**



Signal	Pin	Pin	Signal
1P8V	1	2	1P8V
RXI SO DATA N[0]	3	4	RXI SO DATA N[1]
RXI SO DATA P[0]	5	6	RXI SO DATA P[1]
RXI SO DATA N[2]	7	8	RXI SO DATA N[3]
RXI SO DATA P[2]	9	10	RXI SO DATA P[3]
GND	11	12	GND
RXI SO DATA N[4]	13	14	RXI SO DATA N[5]
RXI SO DATA P[4]	15	16	RXI SO DATA P[5]
RXI SO DATA N[6]	17	18	RXI SO DATA N[7]
RXI SO DATA P[6]	19	20	RXI SO DATA P[7]
GND	21	22	GND
RXI SO LCLK N	23	24	RXI SO FRAME N
RXI SO LCLK P	25	26	RXI SO FRAME P
RXO SO RD WAIT N	27	28	RXO SO WR WAIT N
RXO SO RD WAIT P	29	30	RXO SO WR WAIT P
GND	31	32	GND
TXO SO FRAME N	33	34	TXI SO WR WAIT N
TXO SO FRAME P	35	36	TXI SO WR WAIT P
TXO SO LCLK N	37	38	TXI SO RD WAIT N
TXO SO LCLK P	39	40	TXI SO RD WAIT P
GND	41	42	GND
TXO SO DATA N[0]	43	44	TXO SO DATA N[1]
TXO SO DATA P[0]	45	46	TXO SO DATA P[1]
TXO SO DATA N[2]	47	48	TXO SO DATA N[3]
TXO SO DATA P[2]	49	50	TXO SO DATA P[3]
GND	51	52	GND
TXO SO DATA N[4]	53	54	TXO SO DATA N[5]
TXO SO DATA P[4]	55	56	TXO SO DATA P[5]
TXO SO DATA N[6]	57	58	TXO SO DATA N[7]
TXO SO DATA P[6]	59	60	TXO SO DATA P[7]

**Table 15: PEC\_SOUTH Pin Mapping for Parallella-16**

Signal	Pin	Pin	Signal
1P8V	1	2	1P8V
RXI SO DATA N[7]	3	4	RXI SO DATA N[6]
RXI SO DATA P[7]	5	6	RXI SO DATA P[6]
RXI SO DATA N[5]	7	8	RXI SO DATA N[4]
RXI SO DATA P[5]	9	10	RXI SO DATA P[4]
GND	11	12	GND
RXI SO DATA N[3]	13	14	RXI SO DATA N[2]
RXI SO DATA P[3]	15	16	RXI SO DATA P[2]
RXI SO DATA N[1]	17	18	RXI SO DATA N[0]
RXI SO DATA P[1]	19	20	RXI SO DATA P[0]
GND	21	22	GND
RXI SO LCLK N	23	24	RXO SO RD WAIT N
RXI SO LCLK P	25	26	RXO SO RD WAIT P
TXI SO WR WAIT N	27	28	TXI SO RD WAIT N
TXI SO WR WAIT P	29	30	TXI SO RD WAIT P
GND	31	32	GND
RXI SO FRAME N	33	34	RXO SO WR WAIT N
RXI SO FRAME P	35	36	RXO SO WR WAIT P
TXO SO LCLK N	37	38	TXO SO FRAME N
TXO SO LCLK P	39	40	TXO SO FRAME P
GND	41	42	GND
TXO SO DATA N[7]	43	44	TXO SO DATA N[6]
TXO SO DATA P[7]	45	46	TXO SO DATA P[6]
TXO SO DATA N[5]	47	48	TXO SO DATA N[4]
TXO SO DATA P[5]	49	50	TXO SO DATA P[3]
GND	51	52	GND
TXO SO DATA N[3]	53	54	TXO SO DATA N[2]
TXO SO DATA P[3]	55	56	TXO SO DATA P[2]
TXO SO DATA N[1]	57	58	TXO SO DATA N[0]
TXO SO DATA P[1]	59	60	TXO SO DATA P[0]

**Table 16: PEC\_SOUTH Pin Mapping for Parallella-64**

## 8 Electrical and Performance Specifications

### 8.1 Dimensions and Weight

Feature	
Size	3.4" x 2.15"
Height (with RJ45 and PECs)	1.25"
Height (without RJ45, PECs, 5V DC)	0.75"
PCB Layers	12
PCB Thickness	0.62"
Weight	36 grams

**Table 17: Dimensions and Weight**

### 8.2 Power Consumption

The following table will contain the power consumption for typical Parallella use cases.

	5V_IN	1P0V	1P8V	3P3V	2P5V	VDD_DSP	1P35	VDD_ADJ	VDD_GPIO
Idle	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
Boot	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
Nominal	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
Max	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

**Table 18: Power Consumption**

### 8.3 Performance Metrics

The following table shows the performance specifications of the Parallella board at the time of publication of this reference manual. Give more time for optimization and testing most of these metrics should improve.

Performance Goal	Value
Peak Zynq Frequency	667MHz
Peak Epiphany Instruction Issue Rate	19.2 GIPS (Parallella-16) 76 GIPS (Parallella-64)
Peak Epiphany Frequency	600 MHz (Parallella-16) 600 MHz (Parallella-64)
Peak Floating Point Performance	25 GFLOPS (Parallella-16)

	85 GFLOPS (Parallella-64)
Peak Bandwidth between Zynq and Epiphany	1.3GB/s
PEC_FPGA Peak Bandwidth	2.85GB/s (22.8 Gbps)
PEC_NORTH/PEC_SOUTH Peak Bandwidth	2.6GB/s (25.6 Gbps)

**Table 19: Parallella Performance Summary**

#### 8.4 IC Metrics Summary

Device	Part Number	Power (W)	Temp (C)	$\Theta_{JA}$ (0 m/s)	ESD	Pb-Free
CPU	<a href="#">Zynq™-7000 AP SoC</a>	0.5 – 3	0 – 85°	19.0	1kV HBM	Yes
Epiphany DSP	<a href="#">E16G301</a>	0.4 - 2	0 – 85°	22.6	n/a	Yes
Eth PHY	88E1318 (n/a)	0.5	0 – 125°	37.5	n/a	Yes
USB PHY	<a href="#">USB3320C-EZK-TR</a>	0.1	0 – 85°	n/a	8kV HBM	Yes
HDMI PHY	<a href="#">ADV7513BSWZ</a>	0.3	0 – 85°	43	n/a	Yes
SDRAM	<a href="#">MT41K256M32SLD</a>	0.9	0 – 95° (case)	n/a	n/a	Yes
Flash	<a href="#">N25Q128A13EF840E</a>	0.06	0 – 85° (amb)	n/a	2kV HBM	Yes
PMIC #1	<a href="#">ISL9307</a>	0.2 - 1.5	0 – 125°	40.2	3.5kV HBM	Yes
PMIC #2	<a href="#">ISL9305</a>	0.2 - 1.5	0 – 125°	40.2	3.5kV HBM	Yes
Logic Buffer	<a href="#">NC7WZ16</a>	0.3*	0 – 125°	425	4kV HBM	???
Logic Buffer	<a href="#">NC7SZ125M5X</a>	0.15*	0 – 125°	425	n/a	???
Supply Monitor	<a href="#">STM6904TWEDS6F</a>	~0	0 – 85°	146	n/a	Yes
LVDS Receiver	<a href="#">SN65LVDS4R</a>	0.04	0 – 85° (amb)	171	2kV HBM	Yes
Clock Driver	<a href="#">SI51219-A14BFT</a>	~0	0 – 125°	181	4K HBM	Yes
HDMI Protection	<a href="#">TPD12S016PWR</a>	~0	0 – 85° (amb)	n/a	2K HBM	Yes

**Table 20: IC Metrics**

## 9 About the Parallella Board

### 9.1 Design Information

The board is open source hardware and the Parallella project provides all the files required to study, modify and manufacture the design.

The design resources provided include:

- Complete reference manual
- Schematic sources in OrCAD format
- PCB layout sources in Allegro format
- PCB manufacturing files in Gerber format
- Assembled board 3D CAD model(s)
- Bill of material

Design files for this board will be available at:

<http://github.com/parallella/parallella-hw>

### 9.2 Build Options

The following Parallella assembly options will be supported in manufacturing:

- **Zynq Device:** Z-7010 or Z-7020
- **Epiphany Device:** E16G301 or E64G401
- **IO:** With or without Samtec expansion connectors
- **Display/USB:** With or without HDMI and USB port

### 9.3 Contributors

- **Adapteva: (<http://www.adapteva.com>)**
  - Parallella architecture and board design (Andreas Olofsson)
  - Reference manuals (Andreas Olofsson)
  - FPGA design (Roman Trogan, Fred Huettig)
  - Linux distribution (Roman Trogan, Andreas Olofsson)
  - Board bringup (Roman Trogan, Andreas Olofsson)
- **Boston Design Solutions: (<http://www.bostondesignsolutions.com/>)**
  - Schematic and board layout (Mike Bakhtiari and Mike Damiano)
  - Board bringup/debugging (Joe Galibois)
- **Ant Micro: (<http://www.antmicro.com/>)**
  - HDMI bringup/debugging (Karol Gugala and Peter Gielda)
  - Linux distribution (Karol Gugala)
- **Community Review and Feedback:**
  - Andrew Back
  - Flemming Christensen
  - Gunnar Hillerström
  - @trioflex
  - @tschaboo
  - @hamster
  - @psupine
  - @tnt

## 9.4 Attributions

- Warranty notice and Disclaimers based on those found in the Beaglebone Black System Reference Manual Rev A5.2, authored by Gerald Coley of Texas Instruments and published under the Creative Commons Attribution Share-Alike 3.0 Unported License.
- The Parallella project benefited greatly from being able to study the design of the following open source hardware projects:
  - Arduino
  - Beaglebone
- The Parallella project also drew inspiration from the following projects:
  - Zedboard
  - Raspberry Pi

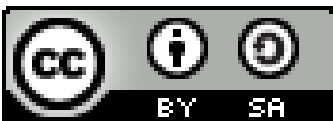
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Send all comments and errors concerning this document to [andreas@adapteva.com](mailto:andreas@adapteva.com)



## 9.6 Disclaimers

These design materials referred to in this document are **\*NOT SUPPORTED\*** and **DO NOT** constitute a reference design. Only “community” support is allowed via resources at <http://forums.parallella.org>

THERE IS NO WARRANTY FOR THE DESIGN MATERIALS DESCRIBED IN THIS REFERENCE MANUAL, TO THE EXTENT PERMITTED BY APPLICABLE LAW. EXCEPT WHEN OTHERWISE STATED IN WRITING THE COPYRIGHT HOLDERS AND/OR OTHER PARTIES PROVIDE THE DESIGN MATERIALS “AS IS” WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. THE ENTIRE RISK AS TO THE QUALITY AND PERFORMANCE OF THE DESIGN MATERIALS IS WITH YOU. SHOULD THE DESIGN MATERIALS PROVE DEFECTIVE, YOU ASSUME THE COST OF ALL NECESSARY SERVICING, REPAIR OR CORRECTION

This Parallella board was designed as an evaluation and development tool. It was not designed with any other application in mind. As such, these design materials may or may not be suitable for any other purposes. If used, the design material becomes your responsibility as to whether or not it meets your specific needs or your specific applications and may require changes to meet your requirements.

For Feasibility Evaluation Only, in Laboratory/Development Environments: The Parallella Board is not a complete product. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk you acknowledge, represent, and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the Parallella for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the Parallella. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the Parallella and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
3. Since the Parallella is not a completed product, it may not meet all applicable regulatory and safety compliance standards which may normally be associated with similar items. You assume full responsibility to determine and/or assure compliance with any such standards and related certifications as may be applicable. You will employ reasonable safeguards to ensure that your use of the Parallella will not result in any property damage, injury or death, even if the Parallella should fail to perform as described or expected.



**Certain Instructions:** It is important to operate the Parallella within Supplier's recommended specifications and environmental considerations per the user guidelines. Exceeding the specified Parallella ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact the Supplier representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the Parallella and/or interface electronics. Please consult the System Reference Manual prior to connecting any load to the Parallella output. If there is uncertainty as to the load specification, please contact the Supplier representative. During normal operation, some circuit components may have case temperatures greater than 60 C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the Parallella schematic located at the link in the Parallella System Reference Manual. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use the Parallella.

**Agreement to Defend, Indemnify and Hold Harmless:** You agree to defend, indemnify and hold the Suppliers, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the Parallella that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the Parallella fails to perform as described or expected.

**Safety-Critical or Life-Critical Applications:** If you intend to evaluate the components for possible use in safety critical applications (such as life support) where a failure of the Supplier's product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify Suppliers of such intent and enter into a separate Assurance and Indemnity Agreement.

## 9.7 Warranty

Parallella.org and Adapteva, Inc (Supplier) provide the Parallella board under the following conditions:

- The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies Supplier from all claims arising from the handling or use of the goods.
- Should the Parallella not meet the specifications indicated in the Parallella Reference Manual, the Parallella may be returned within 90 days from the date of delivery to the distributor of purchase for a full refund.

THE FOREGOING LIMITED WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

For up to date board information, please refer to:

<http://github.com/parallella/parallella-hw>

All support for this board is provided via community support at

<http://forums.parallella.org>

Before returning the board, please request an RMA at:

[www.parallella.org/support/rma](http://www.parallella.org/support/rma)

Please DO NOT return the board without approval from the Parallella RMA team first. All boards received without RMA approval will not be worked on.