C4H10P600A

Power GaN transistor

Rev. 2 — 2 September 2022

AMPLEON

Product data sheet

1. Product profile

1.1 General description

600 W GaN packaged asymmetric Doherty power transistor for base station applications at frequencies from 700 MHz to 1000 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in a Doherty application demo circuit, unless otherwise specified.

Test signal	I_{Dq} (mA)	V_{DS} (V)	$V_{GS(amp)peak}$ (V)	$P_{L(AV)}$ (dBm)	G_p (dB)	η_D (%)	ACPR (dBc)	$P_{L(5dB)}$ (dBm)
f = 791 MHz to 821 MHz								
1-carrier W-CDMA [1]	100	48	–5.7	49.4	18.7	62.4	–24.4	-
pulsed CW [2]	100	48	–5.7	-	-	-	-	58.0
f = 869 MHz to 960 MHz								
1-carrier W-CDMA [1]	180	50	–5.5	50.2	18.0	59.7	–23.9	-
pulsed CW [2]	180	50	–5.5	-	-	-	-	58.1

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 10.5 dB at 0.01 % probability on CCDF.

[2] Test signal: pulsed CW; t_p = 30 μs; δ = 35 %.

1.2 Features and benefits

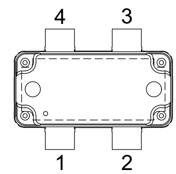
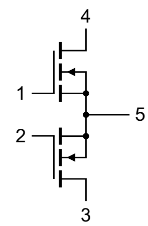
- Excellent digital pre-distortion capability
- High efficiency
- Designed for broadband operation
- Lower output capacitance for improved performance in Doherty applications
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- RF power amplifier for base stations and multi carrier applications in the 700 MHz to 1000 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	gate1 (main)		 amp01358
2	gate2 (peak)		
3	drain2 (peak)		
4	drain1 (main)		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Package name	Orderable part number	12NC	Packing description	Min. orderable quantity (pieces)
OMP-780-4F-1	C4H10P600AY	9349 605 58518	TR13; 100-fold; 44 mm; dry pack	100

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage	operating	-	52	V
V_{DS}	drain-source voltage	V_{GS} = –8 V	-	150	V
$V_{GS(amp)main}$	main amplifier gate-source voltage		–15	+2	V
$V_{GS(amp)peak}$	peak amplifier gate-source voltage		–15	+2	V
$I_{GF(amp)main}$	main amplifier forward gate current		-	27	mA
$I_{GF(amp)peak}$	peak amplifier forward gate current		-	45	mA
T_{stg}	storage temperature		–65	+150	°C
T_{ch}	active die channel temperature	[1]	-	275	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(s-c)(IR)}$ [1]	thermal resistance from active die surface to case by Infrared measurement	T_{case} = 100 °C; $P_{dis(main)}$ = 48 W; $P_{dis(peak)}$ = 15 W	1.26	K/W
$R_{th(ch-c)(FEA)}$ [2]	thermal resistance from active die channel to case by Finite Element Analysis	T_{case} = 100 °C; $P_{dis(main)}$ = 48 W; $P_{dis(peak)}$ = 15 W	1.53	K/W

[1] Infrared (IR) thermal values are for reference only and cannot be used to determine performance or reliability.

[2] Finite Element Analysis (FEA) thermal values have been used for the online MTF calculator.

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Main device						
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 27 mA	–3.15	–2.55	–1.95	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 50 V; I_D = 540 mA	–3.0	–2.4	–1.8	V
$I_{D(leak)}$	drain leakage current	V_{GS} = –10 V; V_{DS} = 50 V	-	-	6.534	mA
I_{GSS}	gate leakage current	V_{GS} = –8 V; V_{DS} = 0 V	-	-	1.307	mA
Peak device						
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 45 mA	–3.13	–2.53	–1.93	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 50 V; I_D = 900 mA	–3.0	–2.4	–1.8	V
$I_{D(leak)}$	drain leakage current	V_{GS} = –10 V; V_{DS} = 50 V	-	-	10.89	mA
I_{GSS}	gate leakage current	V_{GS} = –8 V; V_{DS} = 0 V	-	-	2.178	mA

Table 7. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 7.2 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 64 DPCH; f_1 = 793.5 MHz; f_2 = 818.5 MHz; RF performance at V_{DS} = 48 V; I_{Dq} = 200 mA; $V_{GS(amp)peak}$ = –5.5 V (typical); T_{case} = 25 °C; unless otherwise specified; in a Doherty production RF test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 83 W	17.0	18.2	-	dB
η_D	drain efficiency	$P_{L(AV)}$ = 83 W	56	61	-	%
RL_{in}	input return loss	$P_{L(AV)}$ = 83 W	-	–16.5	–8	dB
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 83 W	-	–24.4	–18	dBc

Table 8. RF characteristics

Test signal: pulsed CW; t_p = 100 μs; δ = 10 %; f_1 = 791 MHz; f_2 = 821 MHz; RF performance at V_{DS} = 48 V; I_{Dq} = 200 mA; $V_{GS(amp)peak}$ = –5.5 V (typical); T_{case} = 25 °C; unless otherwise specified; in a Doherty production RF test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(4dB)}$	output power at 4 dB gain compression	maximum 4 dB compression	450	570	-	W

7. Test information

7.1 Ruggedness in Doherty operation

The C4H10P600A is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 50 V; I_{Dq1} = 200 mA; V_{GS2} = –5.3 V; P_L = 600 W; test signal: pulsed CW, t_p =100 μs, δ = 10 %; f = 791 MHz in a Doherty production RF test circuit.

7.2 Impedance information

Table 9. Typical impedance of maximum power and drain efficiency

Measured load-pull data (main device); all data measured on a harmonic impedance optimized load-pull fixture; I_{Dq} = 400 mA; V_{DS} = 48 V; test signal: pulsed CW; t_p = 100 μs; δ = 10 %; typical values unless otherwise specified.

f	Z_S [1]	Z_L [1]	P_L [2]		η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(dBm)	(W)	(%)	(dB)
Maximum power load						
703	0.5 – j1.9	3.9 – j0.5	55.7	372	70.8	19.6
728	0.6 – j2.1	3.4 – j0.6	55.6	363	74.2	19.7
737	0.6 – j2.1	3.4 – j1.1	55.6	363	70.9	19.3
746	0.6 – j2.2	3.6 – j0.6	55.6	363	74.7	19.6
758	0.7 – j2.3	3.5 – j0.6	55.5	355	74.1	19.4
780	0.7 – j2.5	3.6 – j0.6	55.4	347	73.2	19.3
791	0.7 – j2.6	3.6 – j0.6	55.6	363	74.9	19.2
803	0.8 – j2.7	4.4 – j0.7	55.4	347	74.6	19.2
821	0.8 – j2.9	3.4 – j0.5	55.4	347	72.3	19.0
869	0.9 – j3.4	3.6 – j0.6	55.4	347	73.6	19.0
894	1.2 – j3.6	4.0 – j1.3	55.2	331	69.9	18.6
925	1.4 – j4.1	4.0 – j1.1	55.3	339	72.2	18.6
945	1.5 – j4.4	3.6 – j1.0	55.2	331	70.5	18.6
960	1.7 – j4.6	3.9 – j1.3	55.2	331	70.6	18.5
Maximum drain efficiency load						
703	0.5 – j1.9	5.7 + j2.0	54.2	263	82.6	21.7
728	0.6 – j2.1	3.7 + j1.5	54.4	275	82.3	21.5
737	0.6 – j2.1	3.7 + j1.2	54.4	275	80.3	21.1
746	0.6 – j2.2	5.1 + j1.9	54.1	257	82.5	21.5
758	0.7 – j2.3	3.9 + j1.8	54.2	263	82.4	21.3
780	0.7 – j2.5	4.4 + j2.2	53.6	229	81.5	21.4
791	0.7 – j2.6	4.5 + j2.2	53.4	219	83.9	21.5
803	0.8 – j2.7	5.2 + j2.7	53.5	224	82.0	21.2
821	0.8 – j2.9	4.7 + j2.3	53.4	219	80.1	21.0
869	0.9 – j3.4	4.5 + j2.0	53.8	240	81.7	21.0
894	1.2 – j3.6	4.5 + j1.6	53.7	234	78	20.7

Table 9. Typical impedance of maximum power and drain efficiency *…continued*

Measured load-pull data (main device); all data measured on a harmonic impedance optimized load-pull fixture; I_{Dq} = 400 mA; V_{DS} = 48 V; test signal: pulsed CW; t_p = 100 μs; δ = 10 %; typical values unless otherwise specified.

f	Z_S [1]	Z_L [1]	P_L [2]		η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(dBm)	(W)	(%)	(dB)
925	1.4 – j4.1	4.9 + j1.8	53.6	229	81.0	20.7
945	1.5 – j4.4	3.7 + j1.8	53.5	224	81.1	20.9
960	1.7 – j4.6	3.6 + j1.4	53.7	234	80.4	20.7

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

Table 10. Typical impedance of maximum power and drain efficiency

Measured load-pull data (peak device); all data measured on a harmonic impedance optimized load-pull fixture; I_{Dq} = 660 mA; V_{DS} = 48 V; test signal: pulsed CW; t_p = 100 μs; δ = 10 %; typical values unless otherwise specified.

f	Z_S [1]	Z_L [1]	P_L [2]		η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(dBm)	(W)	(%)	(dB)
Maximum power load						
703	0.7 – j2.5	2.5 – j1.1	57.1	513	73.1	19.4
728	0.8 – j2.7	2.4 – j1.1	57.0	501	72.6	19.0
737	0.8 – j2.8	2.4 – j1.1	57.1	513	72.5	19.0
746	0.8 – j2.9	2.5 – j1.2	57.1	513	73.1	18.9
758	0.9 – j3.0	2.4 – j1.2	57.1	513	73.5	18.7
780	0.9 – j3.2	2.4 – j1.2	57.0	501	71.6	18.6
791	1.0 – j3.3	2.5 – j1.2	57.1	513	74.0	18.6
803	1.0 – j3.4	2.4 – j1.2	56.9	490	72.3	18.4
821	1.1 – j3.6	2.5 – j1.1	57.0	501	73.4	18.3
869	1.3 – j4.1	2.5 – j1.3	56.9	490	73.1	18.2
894	1.5 – j4.4	2.5 – j1.3	56.9	490	72.8	18.3
925	1.8 – j4.9	2.5 – j1.9	56.8	479	68.4	17.6
945	2.0 – j5.2	2.5 – j1.4	56.8	479	72.9	18.0
960	2.4 – j5.4	2.5 – j1.9	56.8	479	68.6	17.4
Maximum drain efficiency load						
703	0.7 – j2.5	2.2 + j0.8	55.5	355	82.5	21.1
728	0.8 – j2.7	2.2 + j0.8	55.4	347	81.5	20.8
737	0.8 – j2.8	2.4 + j0.8	55.3	339	81.5	21.1
746	0.8 – j2.9	2.7 + j0.9	55.4	347	82.2	21.0
758	0.9 – j3.0	2.6 + j1.0	55.1	324	81.8	20.8
780	0.9 – j3.2	2.2 + j0.6	55.4	347	79.0	20.2
791	1.0 – j3.3	2.7 + j1.0	55.1	324	82.6	20.6
803	1.0 – j3.4	2.1 + j0.6	55.3	339	80.3	20.0
821	1.1 – j3.6	2.7 + j0.9	55.1	324	81.3	20.4
869	1.3 – j4.1	3.6 + j0.9	54.9	309	80.9	20.6

Table 10. Typical impedance of maximum power and drain efficiency *…continued*

Measured load-pull data (peak device); all data measured on a harmonic impedance optimized load-pull fixture; I_{Dq} = 660 mA; V_{DS} = 48 V; test signal: pulsed CW; t_p = 100 μs; δ = 10 %; typical values unless otherwise specified.

f	Z_S [1]	Z_L [1]	P_L [2]		η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(dBm)	(W)	(%)	(dB)
894	1.5 – j4.4	2.9 + j0.5	55.2	331	79.2	20.3
925	1.8 – j4.9	3.0 + j0.6	54.9	309	79.1	20.3
945	2.0 – j5.2	2.4 + j0.6	54.7	295	80.3	20.2
960	2.4 – j5.4	2.5 + j0.7	54.5	282	80.2	20.3

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

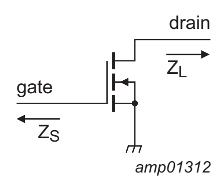
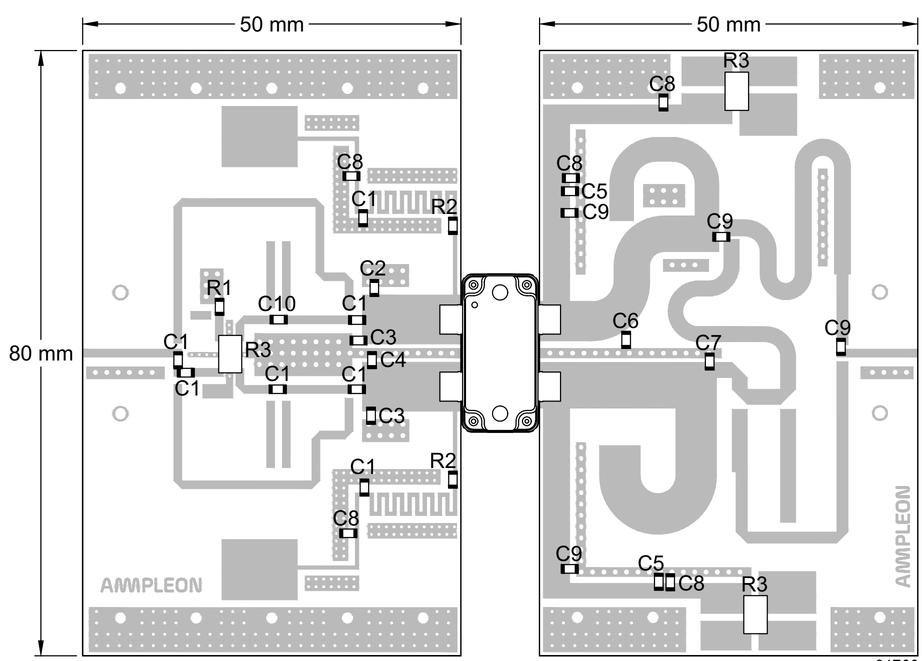


Fig 1. Definition of transistor impedance

7.3 Test circuit



Printed-Circuit Board (PCB): Rogers RO4350B; thickness = 0.508 mm.
See Table 11 for a list of components.

Fig 2. Component layout for test circuit

Table 11. List of components

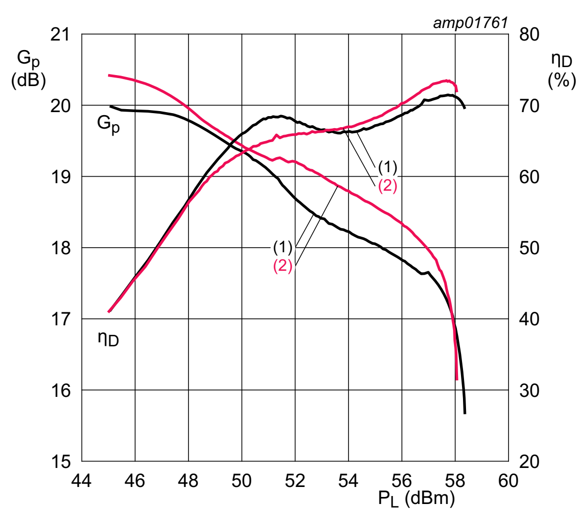
See Figure 2 for component layout.

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	180 pF	ATC 600F
C2	multilayer ceramic chip capacitor	9.1 pF	ATC 600F
C3	multilayer ceramic chip capacitor	10 pF	ATC 600F
C4	multilayer ceramic chip capacitor	11 pF	ATC 600F
C5	multilayer ceramic chip capacitor	1000 pF	ATC 800B
C6	multilayer ceramic chip capacitor	1 pF	ATC 800B
C7	multilayer ceramic chip capacitor	1.5 pF	ATC 800B
C8	electrolytic capacitor	10 μF, 100 V	
C9	multilayer ceramic chip capacitor	180 pF	ATC 800B
C10	multilayer ceramic chip capacitor	36 pF	ATC 600F
X10	hybrid coupler	2 dB, 90°	Anaren: X3C07F1-02S
R1	resistor	51 Ω	
R2	resistor	9.1 Ω	
R3	current sense resistor	10 mΩ	LVK25(1224)

7.4 Graphical data

All the data are measured on the Doherty RF test circuit.

7.4.1 Pulsed CW



V_{DS} = 48 V; I_{Dq} = 100 mA; $V_{GS(amp)peak}$ = −5.5 V; t_p = 100 μs; δ = 10 %.

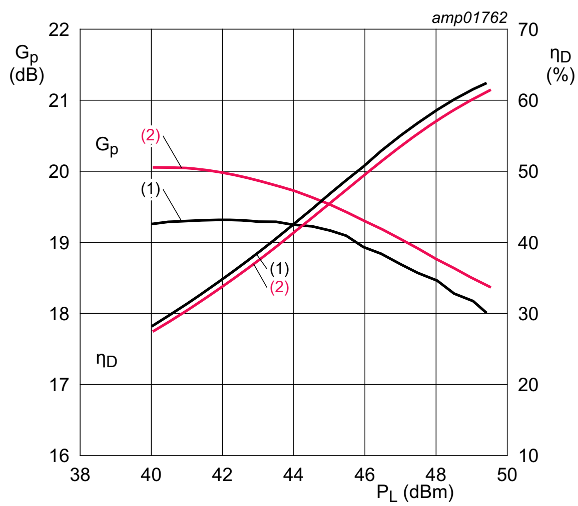
(1) f = 791 MHz

(2) f = 821 MHz

Fig 3. Power gain and drain efficiency as function of output power; typical values

7.4.2 1-Carrier W-CDMA

Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.9 dB at 0.01 % probability on the CCDF.

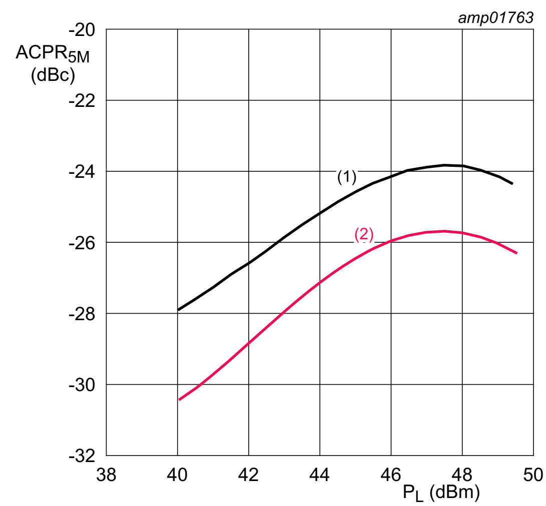


V_{DS} = 48 V; I_{Dq} = 100 mA; $V_{GS(amp)peak}$ = –5.5 V.

(1) f = 791 MHz

(2) f = 821 MHz

Fig 4. Power gain and drain efficiency as function of average output power; typical values

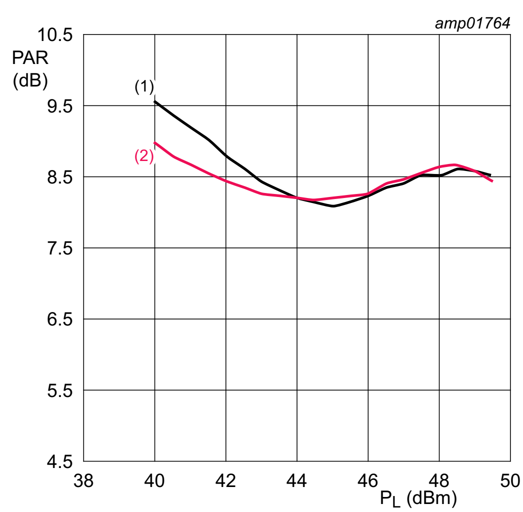


V_{DS} = 48 V; I_{Dq} = 100 mA; $V_{GS(amp)peak}$ = –5.5 V.

(1) f = 791 MHz

(2) f = 821 MHz

Fig 5. Adjacent channel power ratio (5 MHz) as a function of output power; typical values



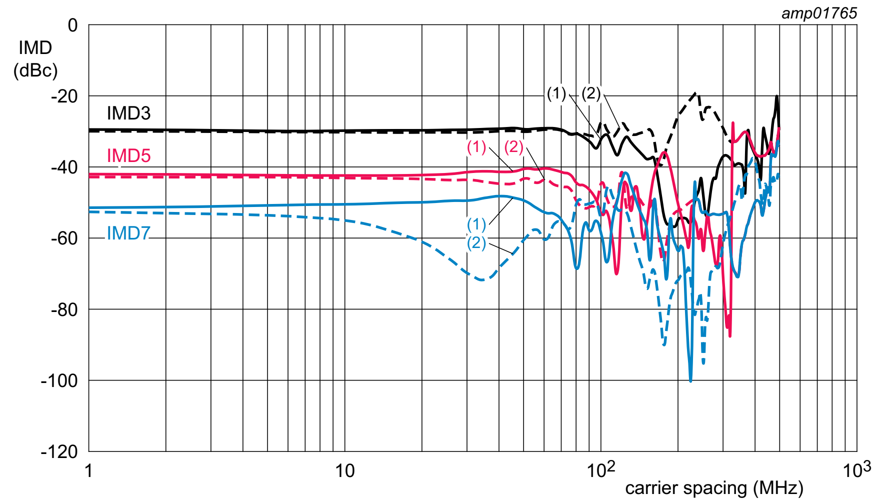
V_{DS} = 48 V; I_{Dq} = 100 mA; $V_{GS(amp)peak}$ = –5.5 V.

(1) f = 791 MHz

(2) f = 821 MHz

Fig 6. Peak-to-average power ratio as a function of output power; typical values

7.4.3 2-Tone VBW



V_{DS} = 48 V; I_{Dq} = 100 mA; $V_{GS(amp)peak}$ = –5.5 V; P_L = 38.2 dBm; f = 806 MHz.

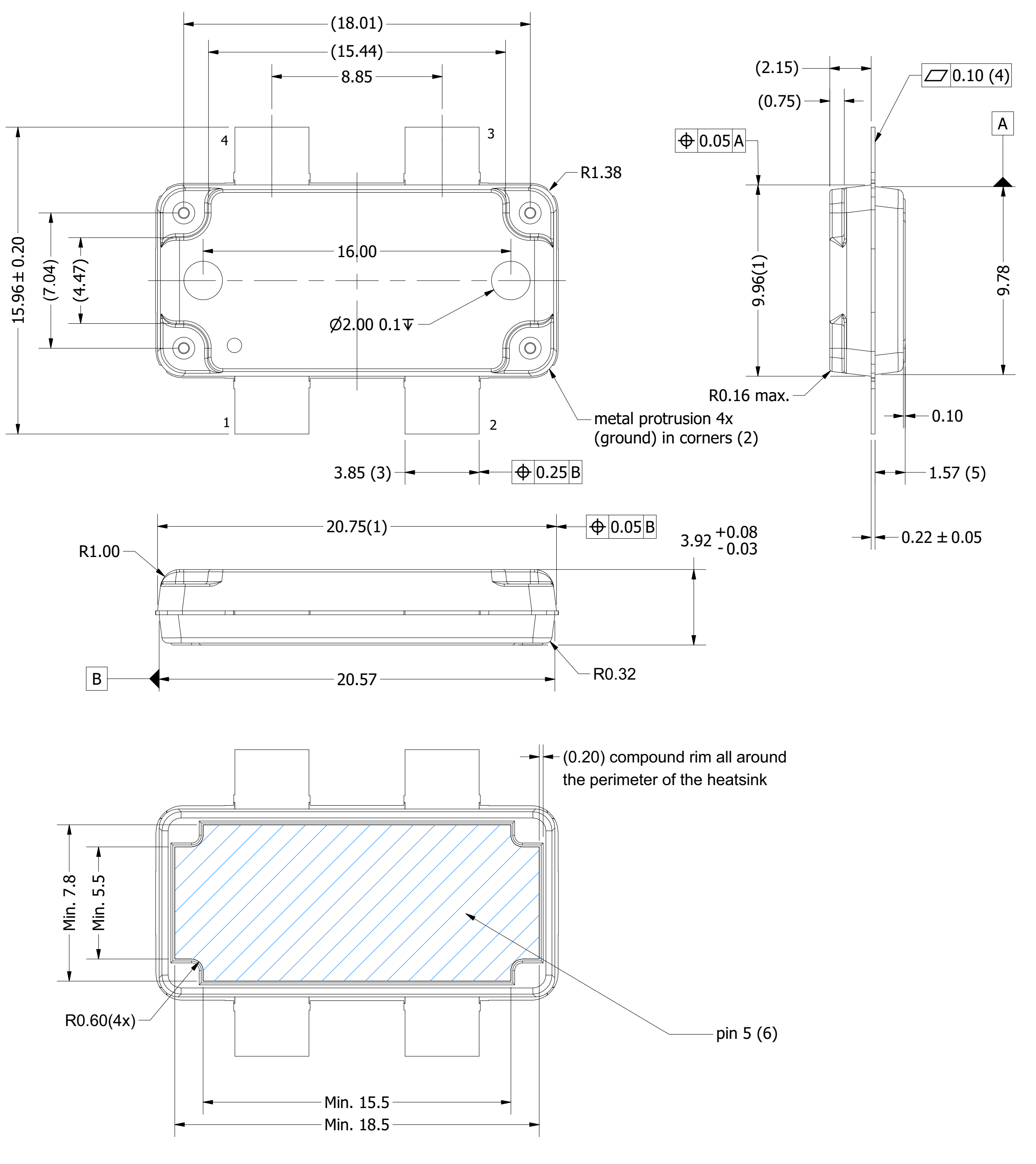
(1) IMD low

(2) IMD high

Fig 7. VBW capability

8. Package outline

OMP-780-4F-1

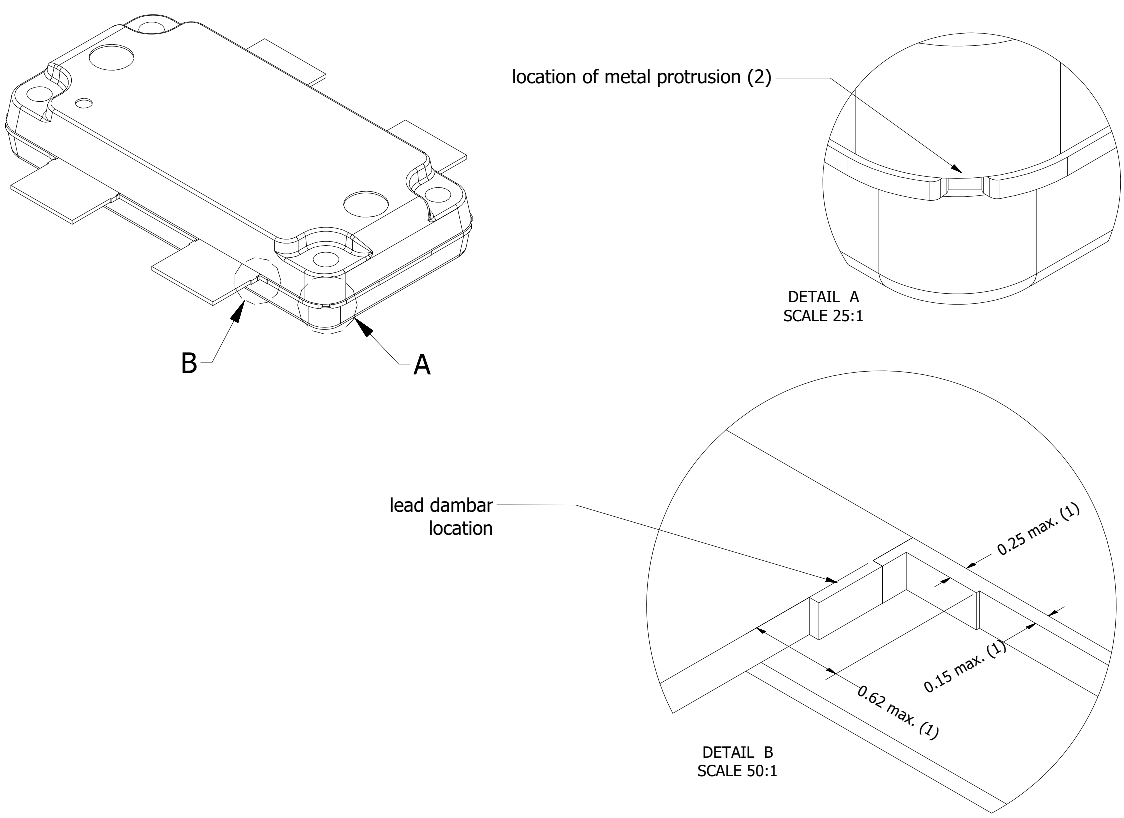


Package outline drawing: OMP-780-4F-1	units in mm.	Tolerances unless otherwise stated: Dimension: ± 0.05 Angle: ± 1°	Revision: 0 Revision date: 3/1/2018
		Third angle projection	Sheet 1 of 2

Fig 8. Package outline OMP-780-4F-1 (sheet 1 of 2)

OMP-780-4F-1

Drawing Notes	
Items	Description
(1)	Dimensions are excluding mold protrusion. All areas located adjacent to the leads have a maximum mold protrusion of 0.25 mm (per side) and max. 0.62 mm in length. At all other areas the mold protrusion is maximum 0.15 mm per side. See also detail B.
(2)	The metal protrusion (tie bars) in the corner will not stick out of the molding compound protrusions (detail A).
(3)	The lead dambar (metal) protrusions are not included. Add 0.14 mm max to the total lead dimension at the dambar location.
(4)	The lead coplanarity over all leads is 0.1 mm maximum.
(5)	Dimension is measured 0.5 mm from the edge of the top package body.
(6)	The hatched area indicates the exposed metal heatsink.
(7)	The leads and exposed heatsink are plated with matte Tin (Sn).



Package outline drawing: OMP-780-4F-1	units in mm.	Tolerances unless otherwise stated: Dimension: ± 0.05 Angle: ± 1°	Revision: 0 Revision date: 3/1/2018
		Third angle projection	Sheet 2 of 2

Fig 9. Package outline OMP-780-4F-1 (sheet 2 of 2)

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 12. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C3 [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	1B [2]

[1] CDM classification C3 is granted to any part that passes after exposure to an ESD pulse of 1000 V.

[2] HBM classification 1B is granted to any part that passes after exposure to an ESD pulse of 500 V.

10. Abbreviations

Table 13. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
GaN	Gallium Nitride
MTF	Median Time to Failure
PAR	Peak-to-Average Ratio
RoHS	Restriction of Hazardous Substances
VBW	Video BandWidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
C4H10P600A v.2	20220902	Product data sheet	-	C4H10P600A v.1
Modifications:	• Table 4 on page 2: table updated • Table 7 on page 3: updated value of $V_{GS(amp)peak}$ in description • Table 8 on page 3: updated value of $V_{GS(amp)peak}$ in description • Section 7.1 on page 4: updated section • Section 7.2 on page 4: updated tables • Figure 2 on page 6: updated value of thickness • Table 11 on page 7: updated components X10 and R1 • Section 7.4 on page 7: added paragraph below title • Figure 7 on page 9: updated notes			
C4H10P600A v.1	20220513	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

12.2 Definitions

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13. Contact information

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