BVA3153

Medium Power Digital Variable Gain Amplifier

3600MHz – 4200MHz

Product Description

The BVA3153 is a digitally controlled variable gain amplifier (DVGA) in a 6m x 6mm LGA package, with a frequency range of 3.6 to 4.2GHz and an operating VDD of 5.0V.

BVA3153 is high performance and high dynamic range makes it ideally suited for use in 5G/LTE wireless infrastructure and other high performance wireless RF applications.

The BVA3153 is an integration of a high performance digital 7-bit attenuator (DSA) that provides a 31.75dB ATT range in 0.25dB steps, and high linearity broadband gain block amplifiers featuring high ACP and P1dB.

The BVA3153 digital control interface supports serial programming of the attenuator, and includes the reference gain (max gain, bypass) state on the Parallel programing .

The BVA3153 is integrated of two gain blocks (AMP1, AMP2), a digital step attenuator (DSA) and high linearity amplifier (AMP3).

Implementation requires only a few external components, such as matching capacitors on the Input and Output pins. (Don't need DC Blocking Capacitor)

This device is packaged in a 28-pin LGA, 6mm x 6mm x 0.95mm with 50Ω single-ended RF input and RF output impedances for ease of integration into the signal-path.

Figure 1. Functional Block Diagram

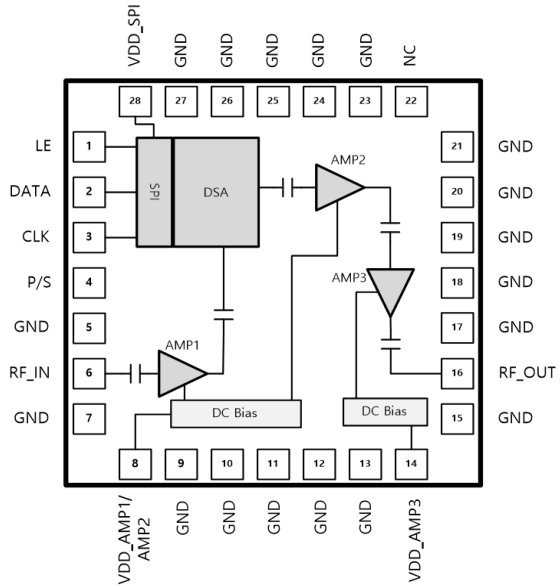


Figure 2. Package Type

28-pin 6mm x 6mm x 0.95mm LGA

Device Features

- 28-Pin 6mm x 6mm x 0.95mm LGA Package
- Integrated AMP1 + DSA + AMP2 + AMP3
- A Single +5.0V supply
- 3.6 - 4.2GHz Frequency Range
- 38.5dB Gain @ 3.9GHz
- 4.0dB Noise Figure @ 3.9GHz (Max Gain)
- 26.7dBm Output P1dB @ 3.9GHz
- 43dBm Output IP3 @ 3.9GHz
- ACP at 3.95GHz
  5G NR 100MBW (±100MHz offset) ≥ 15.0dBm
  5G NR 100MBW (±100MHz offset) @ 10dBm Output ≥ 56.5dBc
- Attenuation Range
  0.25 dB step up to 31.75 dB
- Glitch-less attenuation state transitions
- High attenuation accuracy
  ±(0.25dB + 5% x ATT Settings) @ 3.6 - 4.2GHz
- Programming Interface
  Serial / Parallel (Bypass Mode)
- Lead-free/RoHS2-compliant SiP LGA SMT Package

Application

- 5G/4G/3G wireless Infrastructure
- Small Cells
- Repeaters

Table 1. Electrical Specifications

Typical Performance Data @ 25°and VDD = 5.0V, ATT=0dB state (Max. gain) unless otherwise noted.
(De-embedded PCB and connector Loss)

Parameter		Condition	Min	Typ	Max	Unit
Operational Frequency Range			3600		4200	MHz
Gain		@ ATT = 0dB, 3.9GHz	36	38.5	41	dB
Gain Flatness		3.8GHz to 4.0GHz ATT = 0dB		0.3		dB
		3.6GHz to 4.2GHz ATT = 0dB		1.0		dB
Attenuation Control range		0.25dB step		0 - 31.75		dB
Attenuation Step				0.25		dB
Attenuation Accuracy		Any bit or bit combination	−(0.25 +5% of ATT. setting)		+ (0.25 +5% of ATT. setting)	dB
Return loss	**Input Return Loss**	ATT = 0dB		15		dB
	Output Return Loss			15		
Output Power for 1dB Compression		@ ATT = 0dB, 3.9GHz		26.7		dBm
Output Third Order Intercept Point		@ ATT = 0dB, 3.9GHz	38	42		dBm
		Pout= +5dBm/tone △f = 1MHz				
Adjacent Channel Leakage Ratio		10dBm Output @3.95GHz 5G NR 100MBW, ATT = 0dB		-56.5		dBc
		10dBm Output @3.95GHz 5G NR 100MBW, ATT = 15dB		-57.5		dBc
Noise Figure		@ ATT = 0dB, 3.9GHz		4		dB
Switching time		50% CTRL to 90% or 10% RF		275		ns
Supply voltage		DSA	3.3	5	5.5	V
		AMP		5		V
Supply Current		AMP1+DSA+AMP2+AMP3	260	310	360	mA
Control Interface		Serial mode		8		Bit
Control Voltage		Digital input high	1.17		3.6	V
		Digital input low	-0.3		0.63	V
Impedance				50		Ω

Table 2. Typical RF Performance[1]

Typical Performance Data @ 25°, Max Gain State and VDD = 5.0V unless otherwise noted. (All data de-embedded PCB and Connector Loss)

Parameter	Frequency					Unit
Frequency	**3.6**	**3.8**	**3.9**	**4.0**	**4.2**	**GHz**
Gain	38.1	38.3	38.5	38.5	37.4	dB
S11	-18	-23	-28	-35	-22	dB
S22	-16	-16	-17	-18	-15	dB
OIP3[2]	41.4	42.8	43	42.6	39.8	dBm
P1dB	26.6	26.4	26.7	26.5	26	dBm
ACP[3]**, ATT=0dB (Max Gain)**	-57	-57	-56.4	-57	-56.1	dBc
ACP[3]**, ATT=15dB**	-57.8	-58.7	-57.9	-57.4	-55.5	dBc
N.F	3.8	4	4	4.2	4.4	dB

[1] Device performance _ measured on a BeRex evaluation board at 25°C, VDD=+5.0V, 50 Ω system. measure on Evaluation Board De-embedded PCB and Connector Loss.

[2] OIP3 _ measured with two tones at an output of +7dBm per tone separated by 1MHz.

[3] 5G set-up: 3GPP 5G NR, 100MHz BW, ±100MHz offset. Output Power 10dBm. Applied the Noise correlation function of Instrument.

Table 3. Absolute Maximum Ratings[1]

Parameter	Min	Typ	Max	Unit
Supply Voltage(VDD)	-0.3		5.5	V
Supply Current			580	mA
Digital input voltage	-0.3		3.6	V
Maximum input power			+20	dBm
Storage Temperature	-55		+150	℃

[1] Operation of this device above any of these parameters may result in permanent damage.

Table 4. Recommended Operating Conditions[1]

Parameter	Min	Typ	Max	Unit
Bandwidth	3600		4200	MHz
Supply Voltage(VDD)	4.85	5	5.15	V
Operating Temperature	-40		+105	˚C
Thermal Resistance (θ_{JC})		23.6		˚C/W

[1] Specifications are not guaranteed over all recommended operating conditions.

Programming Option

Serial / Parallel (Bypass) Selection

Either a Serial or Parallel interface can be used to control the P/S Pin. The P/S bit provides the selection, with P/S = HIGH selecting the Serial interface and P/S = LOW selecting the Parallel interface (Bypass Mode, Max Gain State).

Serial Interface

The Serial interface is an 8-bit Serial-In, Parallel-Out shift register buffered by a transparent latch. The 8-bits make up the Attenuation Word that controls the DSA. Figure 4 illustrates an example timing diagram for programming a state.

The Serial interface is controlled using three CMOS compatible signals: SI, Clock (CLK) and LE. The SI and CLK inputs allow data to be serially entered into the shift register. Serial data is clocked in LSB first.

The shift register must be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data into the DSA. The Attenuation Word truth table is listed in Table 5. A programming example of the serial register is illustrated in Figure 3. The Serial timing diagram is illustrated in Figure 4.

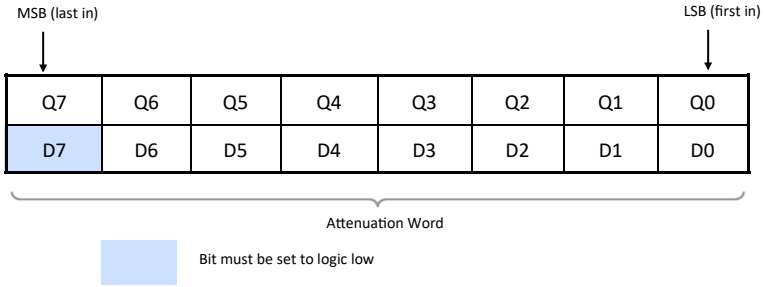
Table 5. Serial Attenuation word Truth Table

Attenuation Word								Attenuation setting
D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)	
L	L	L	L	L	L	L	L	Max. Gain
L	L	L	L	L	L	L	H	0.25 dB
L	L	L	L	L	L	H	L	0.5 dB
L	L	L	L	L	H	L	L	1 dB
L	L	L	L	H	L	L	L	2 dB
L	L	L	H	L	L	L	L	4 dB
L	L	H	L	L	L	L	L	8 dB
L	H	L	L	L	L	L	L	16 dB
L	H	H	H	H	H	H	H	31.75 dB

Power-up Control Settings

The BVA3153 will always initialize to the maximum attenuation setting (Atten=31.75dB) on power-up for the Serial mode and will remain in this setting until the user latches in the next programming word.

Figure 3. Serial Register Map



The attenuation word is derived directly from the value of the attenuation state. To find the attenuation word, multiply the value of the state by four, then convert to binary.

For example, to program the 12.5dB state;

4 x 12.5 = 50
50 → 00110010

Serial Input : 00110010

Figure 4. Serial Interface Timing Diagram

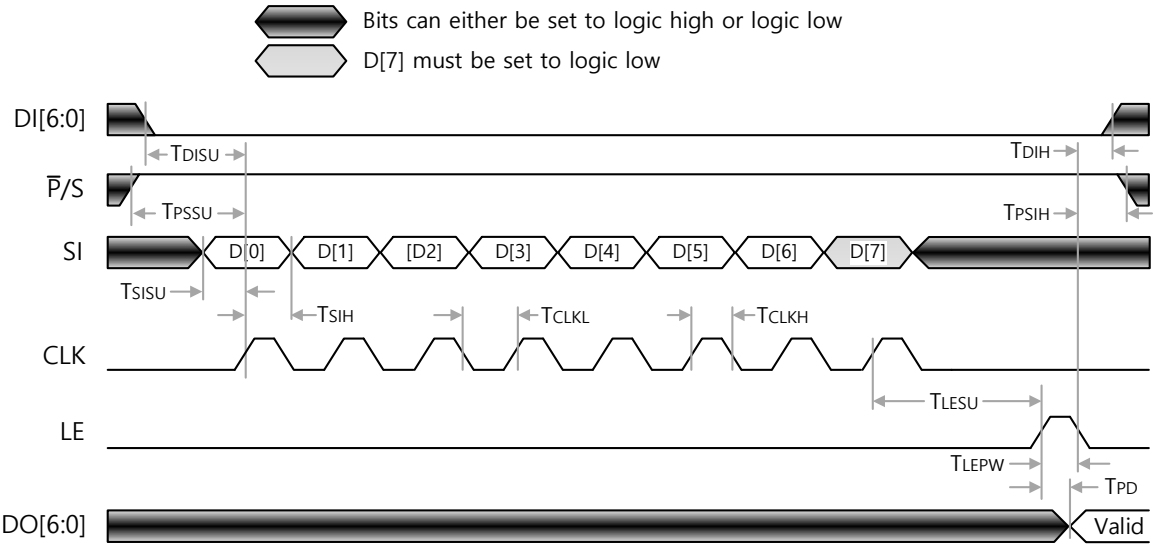


Table 6. Serial Interface AC Characteristics

VDD = 5.0V with DSA only, -40°C ≤ T_A ≤ 105°C, unless otherwise specified

Symbol	Parameter	Min	Max	Unit
F_{CLK}	Serial data clock frequency		10	MHz
T_{CLKH}	Serial clock HIGH time	30		ns
T_{CLKL}	Serial clock LOW time	30		ns
T_{LESU}	Last Serial clock rising edge setup time to Latch Enable rising edge	10		ns
T_{LEPW}	Latch Enable minimum pulse width	30		ns
T_{SISU}	Serial data setup time	10		ns
T_{SIH}	Serial data hold time	10		ns
T_{DISU}	Parallel data setup time	100		ns
T_{DIH}	Parallel data hold time	100		ns
T_{PSSU}	Parallel / Serial setup time	100		ns
T_{PSIH}	Parallel / Serial hold time	100		ns
T_{ASU}	Address setup time	100		ns
T_{AH}	Address hold time	100		ns
T_{PD}	Digital register delay (internal)		10	ns

Figure 5. Pin Configuration

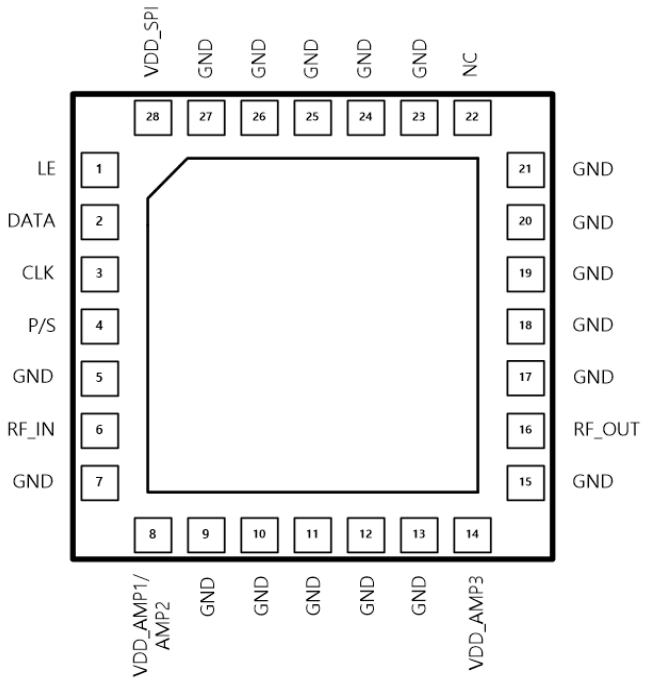


Table 7. Pin Description

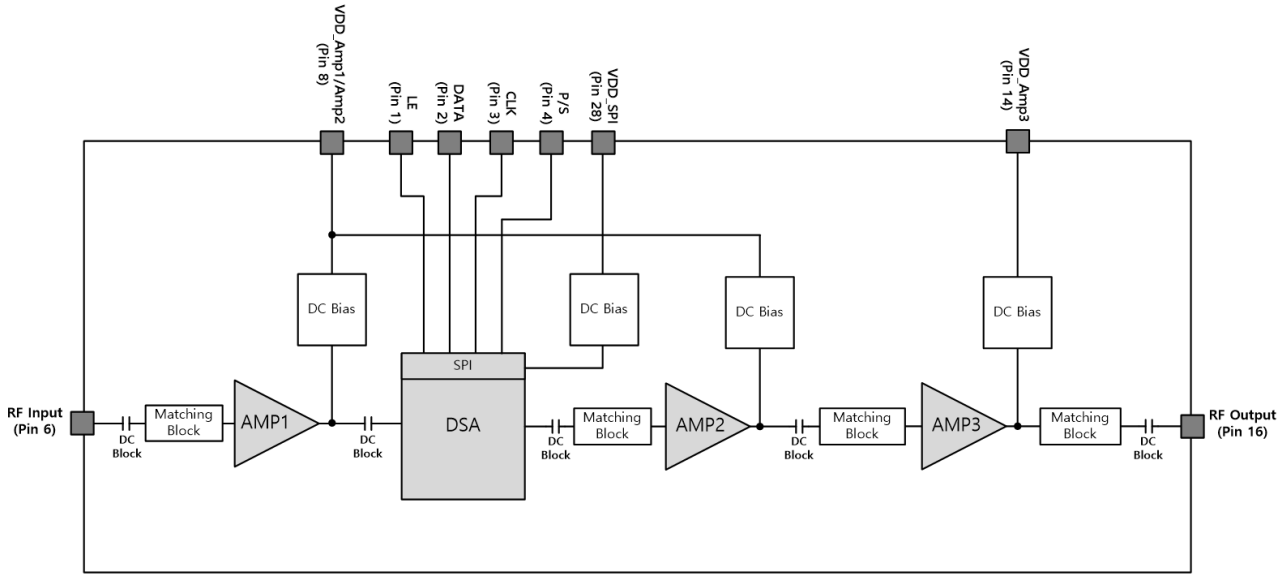
Pin	Pin name	Description
1	LE[1]	Serial Latch Enable Input. When LE is high, latch is clear and content of SPI control the attenuator. When LE is low, data in SPI is latched.
2	DATA	Serial Data Input. The data and clock pins allow the data to be entered serially into SPI and is independent of Latch state.
3	CLK	Serial Clock Input.
4	P/S	The P/S bit provides this selection, P/S=Low selecting the Parallel Interface which is the Max. gain state (Bypass Mode, ATT=0dB) and either P/S=High selecting or floating for the Serial Interface.
6	RF_IN	RF Input, matched to 50 ohm. Internally DC blocked.
8	VDD_AMP1/AMP2	Supply Voltage to AMP1 and AMP2. This pin is connected internally to bypass capacitors followed by inductor inside the module.
14	VDD_AMP3	Supply Voltage to AMP3. This pin is connected internally to bypass capacitors followed by inductor inside the module.
16	RF_OUT	RF output, matched to 50 ohm. Internally DC blocked.
22	NC	No connect or Ground. This pin is not connected.
28	VDD_SPI	SPI and DSA DC supply. This pin is connected to bypass capacitor internally.
5, 7, 9-13, 15 17-21,23-27	GND	RF/DC Ground
Backside Pad	GND	RF/DC Ground

[1]LE must be Pulled-up to 1.17V—3.6V to use the Bypass Mode when P/S = Low (Bypass mode, ATT=0dB)

Figure 6. Internal Function Block Diagram

The BVA3153 is integrated of two gain block (AMP1, AMP2), a digital step attenuator (DSA) and high linearity amplifier (AMP3). Additionally, the BVA3153 includes an internal bias and RF matching circuits to improve the RF performance at 3.6GHz - 4.2GHz.

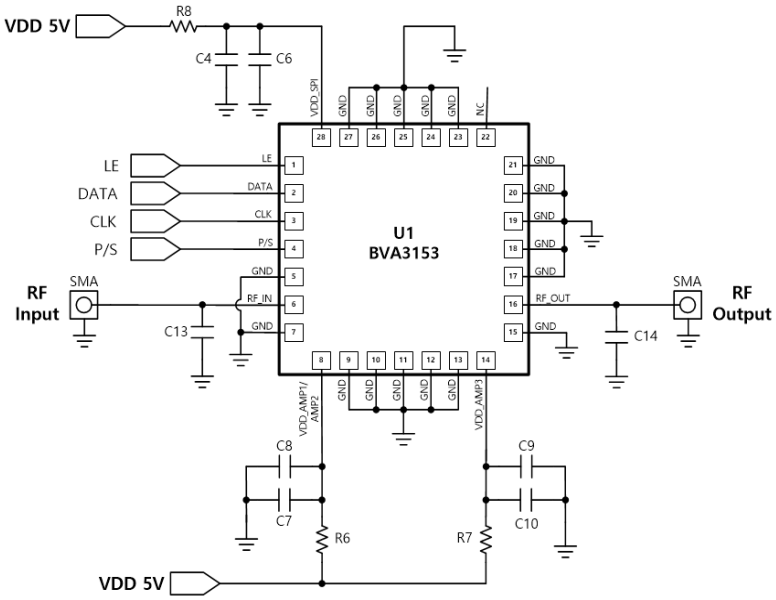
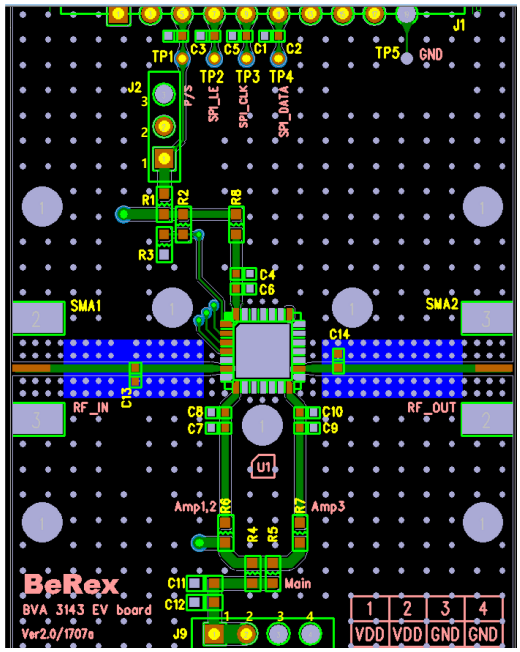
The Internal structure of the Package is shown below.



Typical RF Performance Plot - BVA3153 EVK - PCB

Typical Performance Data @ 25°and VDD = 5.0V unless otherwise noted and RF Circuit

Table 8. Application Circuit

Schematic Diagram	BOM			Remark
	Ref	Size	Value	
	C4	0402	NC	
	C6	0402	100 nF	
	C7	0402	100 nF	
	C8	0402	NC	
	C9	0402	NC	
	C10	0402	100 nF	
	C13	0402	0.3 pF	
	C14	0402	0.7 pF	
	R6	0603	0 Ω	
	R7	0603	0 Ω	
	R8	0603	0 Ω	
	NOTE 1. C1, C2, C3, C5, R1 are NC 2. R2 = 100 KΩ, R3=200 KΩ 3. R4, R5 = 0 Ω 4. C11 = 100pF, C12=1uF 5. J2 Information - Not connected (Floating) : Serial Mode - Connected 1-2 : Serial Mode - Connected 2-3 : Bypass Mode (Max Gain State) 6. J9 Information - Pin 1, 2 : 5Vdc - Pin 3, 4 : Ground			

Typical RF Performance Plot - BVA3153 EVK

Typical Performance Data @ 25°and VDD = 5.0V unless otherwise noted. (All data de-embedded PCB and Connector Loss)

Table 9. Typical Performance : 3.9GHz

Parameter	Typical Values				Units
Frequency	**3.9**	**3.9**	**3.9**	**3.9**	**GHz**
Temperature	-40	25	85	105	℃
Vcc	5	5	5	5	Vdc
Current	290	305	315	312	mA
Gain	39.2	38.5	37.3	36.8	dB
S11	-23	-26	-30	-27	dB
S22	-14	-17	-17	-16	dB
OIP3[1]	42.8	43	40.6	39.3	dBm
P1dB	27.2	26.7	26.4	26.3	dBm
Noise Figure	3.7	4	4.6	4.9	dB
5G NR 100MHz ACP[2]	-56.7	-56.4	-57.3	-57	dBc

[1] OIP3 _ measured with two tones at an output of 7dBm per tone separated by 1 MHz.

[2] 5G NR set-up: 3GPP 5G NR, 100MHz BW, ±100MHz offset. Output Power 10dBm. Applied the Noise correlation function of Instrument.

Figure 7. Gain Flatness

: Max Gain, Temp.

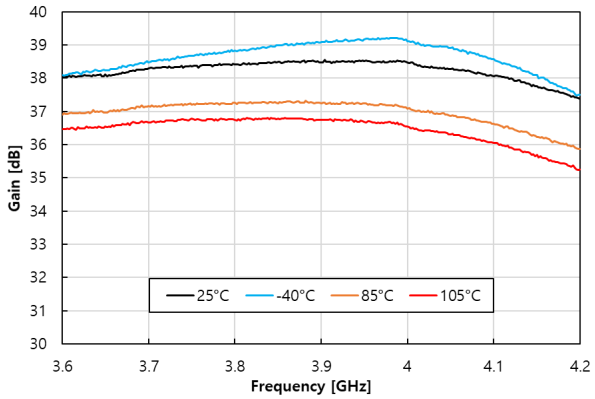


Figure 8. Gain Flatness

: Min Gain, Temp.

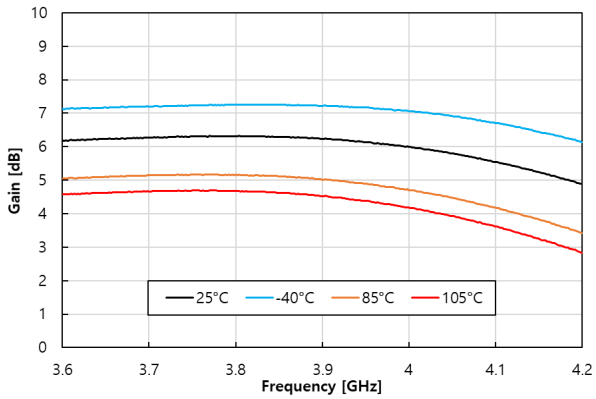


Figure 9. Input Return Loss

: : Max Gain, Temp.

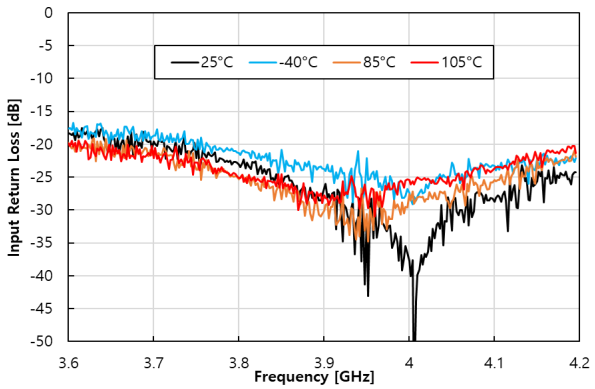
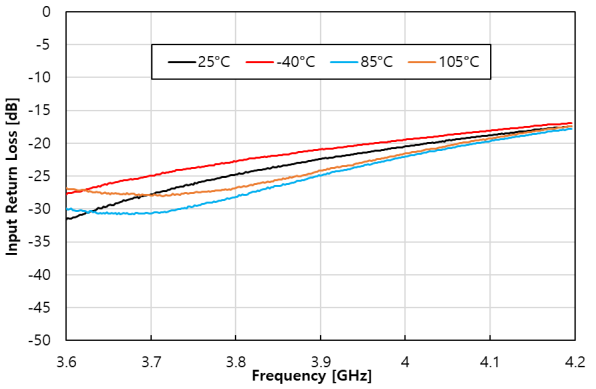


Figure 10. Input Return Loss

: Min Gain, Temp.



Typical RF Performance Plot - BVA3153 EVK

Typical Performance Data @ 25°and VDD = 5.0V unless otherwise noted. (All data de-embedded PCB and Connector Loss)

Figure 11. Output Return Loss

: Max Gain, Temp.

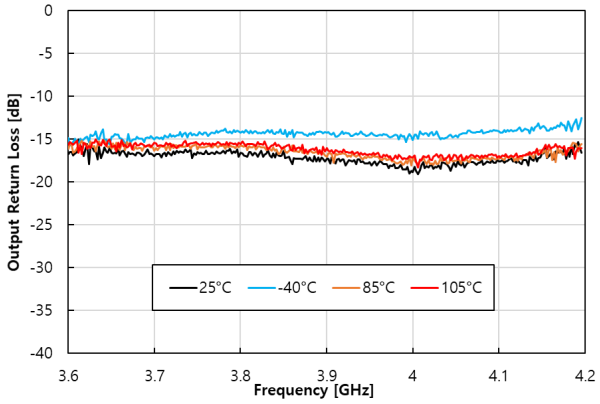


Figure 12. Output Return Loss

: Min Gain, Temp.

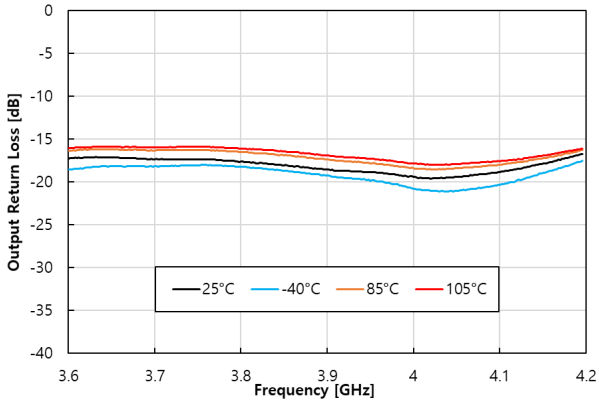


Figure 13. Gain

: Attenuation Setting

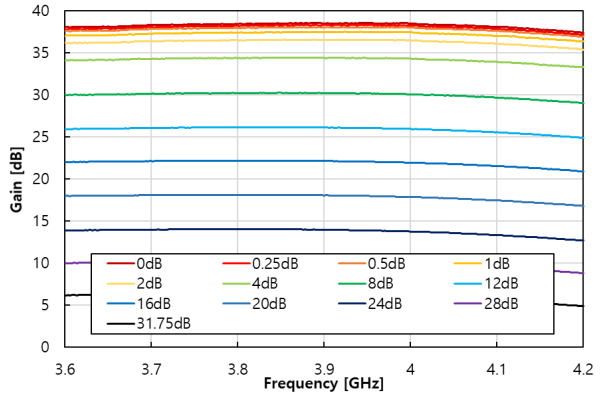


Figure 14. Gain

: Frequency, Attenuation Setting

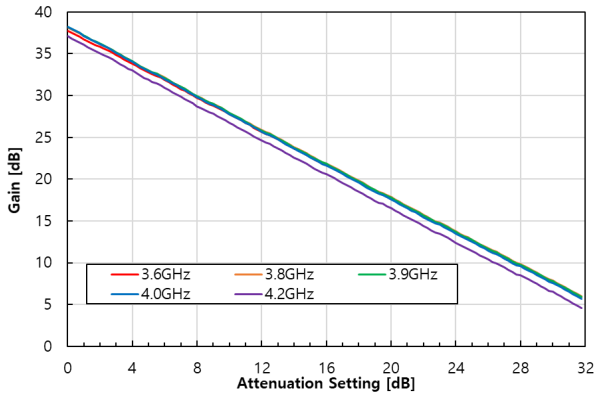
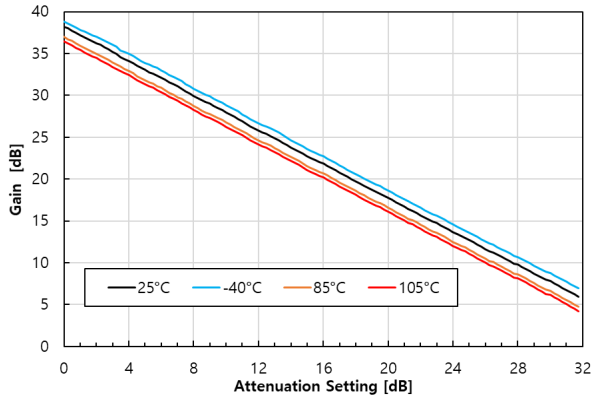


Figure 15. Gain

: 3.9GHz, Attenuation Setting, Temp.



Typical RF Performance Plot - BVA3153 EVK

Typical Performance Data @ 25°and VDD = 5.0V unless otherwise noted. (All data de-embedded PCB and Connector Loss)

Figure 16. Attenuation Error

: 3.9GHz, Temp.

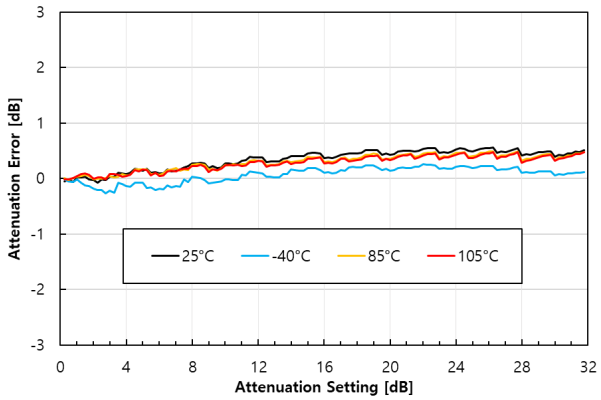


Figure 17. Attenuation Error

: Frequency

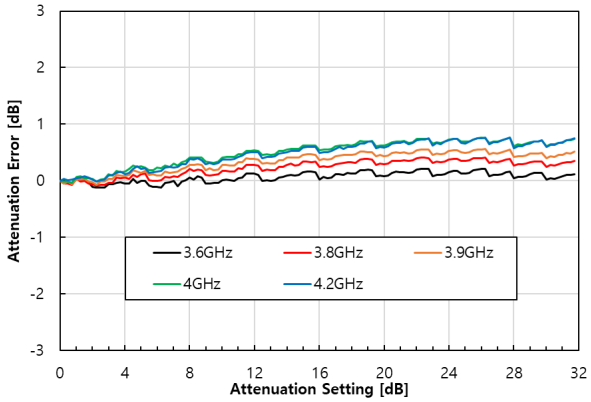
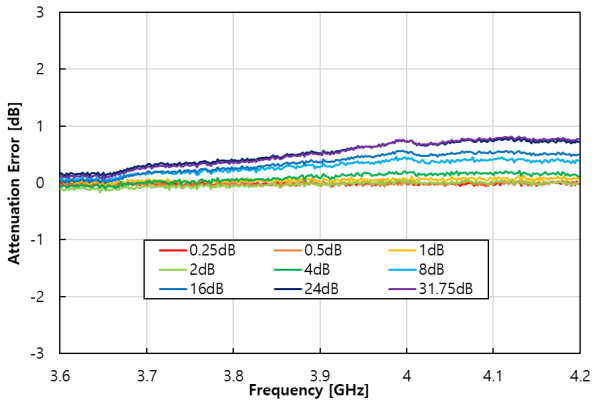


Figure 18. Attenuation Error

: Attenuation Setting



Typical RF Performance Plot - BVA3153 EVK

Typical Performance Data @ 25°and VDD = 5.0V unless otherwise noted. (All data de-embedded PCB and Connector Loss)

Figure 19. OIP3

: Frequency, ATT=0dB, 1MHz interval

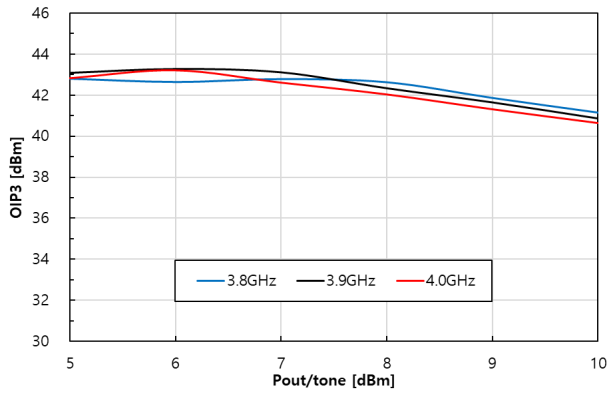


Figure 20. OIP3

: Frequency, ATT=15dB, 1MHz interval

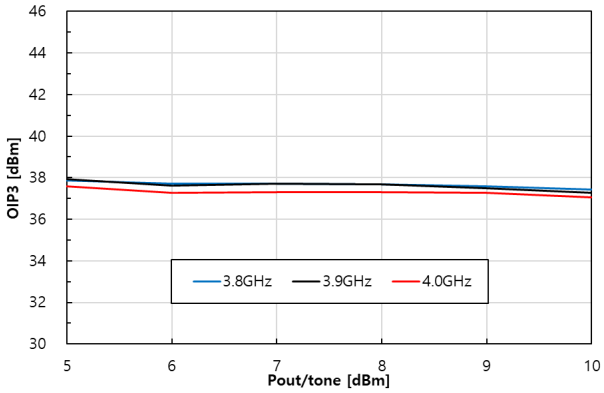


Figure 21. OIP3

: ATT=0dB, Output=7dBm/tone, 1MHz interval, Temp.

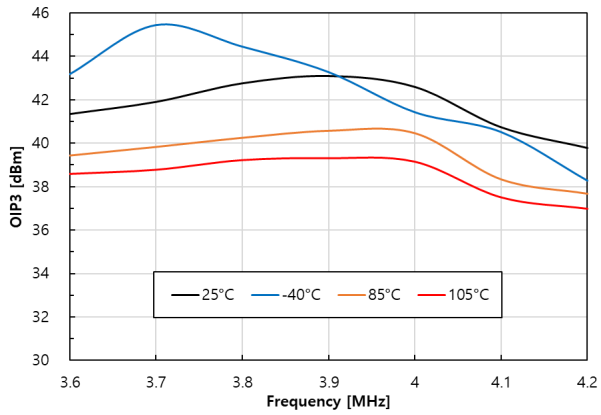


Figure 22. OIP3

: 3.9GHz, ATT=0dB, 1MHz interval, Temp.

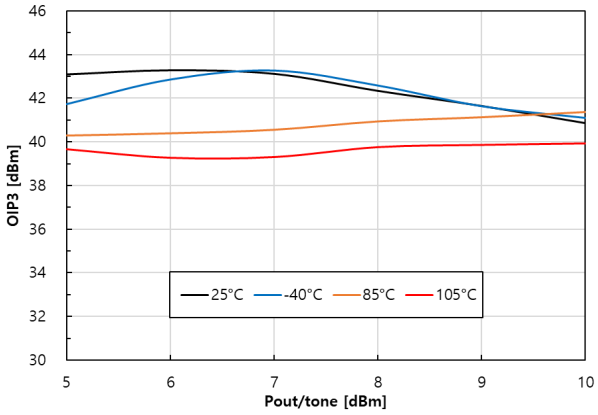


Figure 23. OP1dB

: ATT=0dB, Temp.

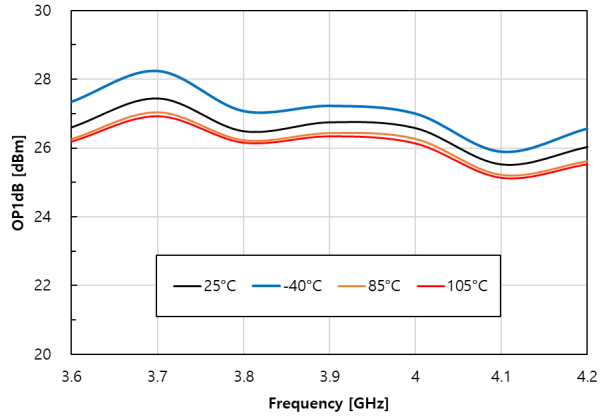
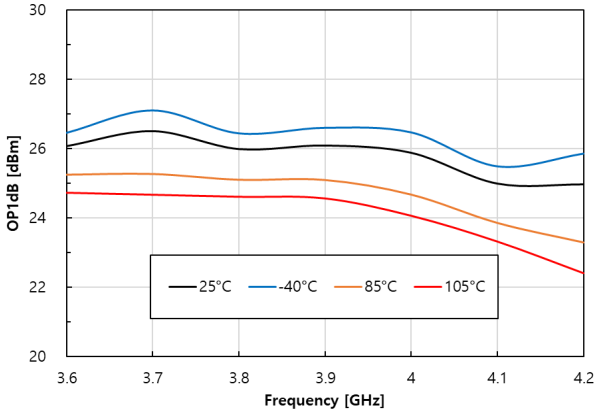


Figure 24. OP1dB

: ATT=15dB, Temp.



Typical RF Performance Plot - BVA3153 EVK

Typical Performance Data @ 25°and VDD = 5.0V unless otherwise noted. (All data de-embedded PCB and Connector Loss)

Figure 25. ACP

: 3.85GHz, ATT = 0dB, 5G NR 100MBW, Temp.

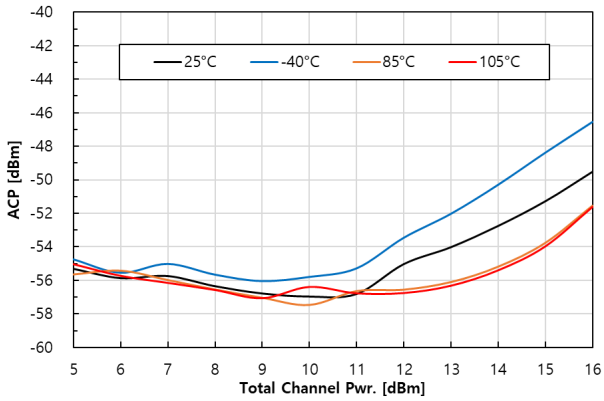


Figure 26. ACP

: 3.85GHz, ATT = 15dB, 5G NR 100MBW, Temp.

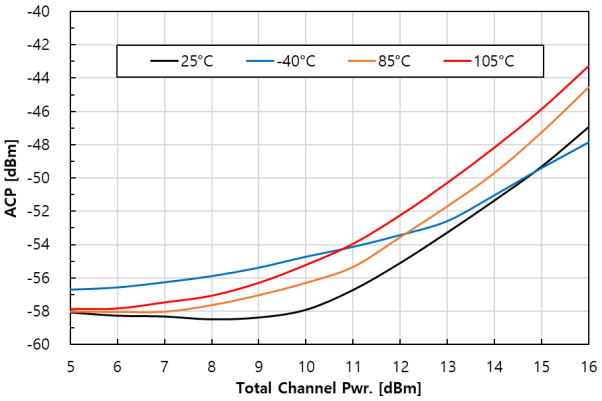


Figure 27. ACP

: 3.95GHz, ATT = 0dB, 5G NR 100MBW, Temp.

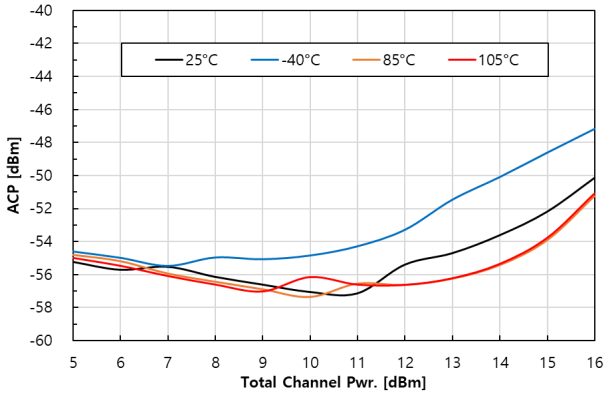


Figure 28. ACP

: 3.95GHz, ATT = 15dB, 5G NR 100MBW, Temp.

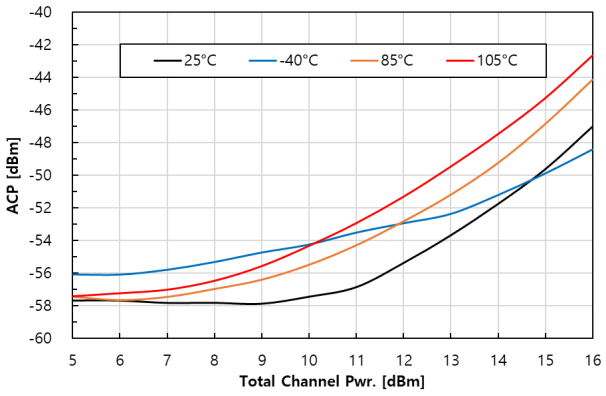


Figure 29. ACP

: Frequency, ATT = 0dB, 5G NR 100MBW

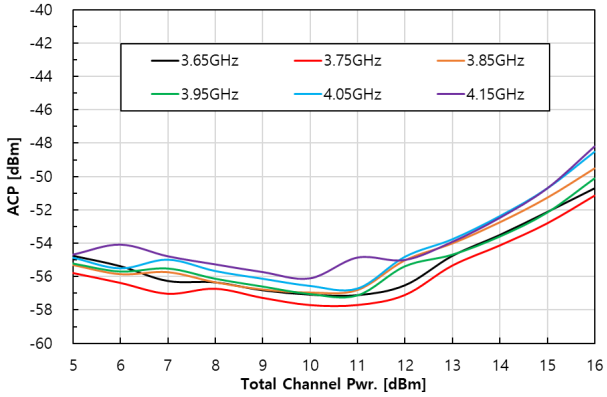
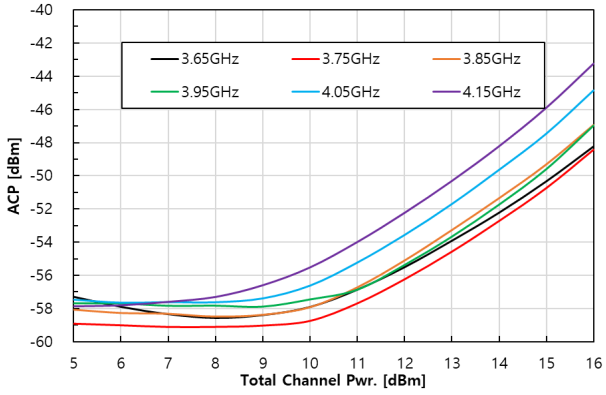


Figure 30. ACP

: Frequency, ATT = 15dB, 5G NR 100MBW



Typical RF Performance Plot - BVA3153 EVK

Typical Performance Data @ 25°and VDD = 5.0V unless otherwise noted. (All data de-embedded PCB and Connector Loss)

Figure 31. Noise Figure

: ATT = 0dB, Temp.

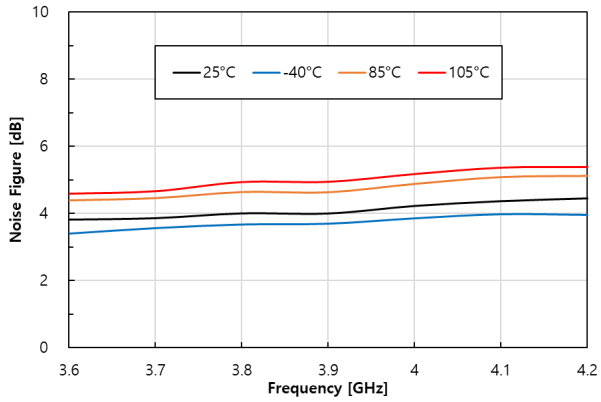


Figure 32. Noise Figure

: ATT = 16dB, Temp.

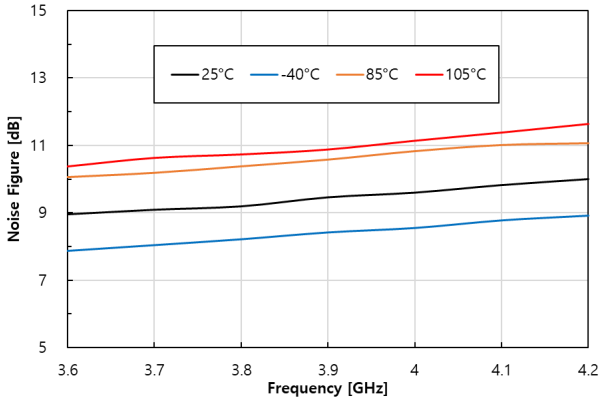


Figure 33. Evaluation Board Schematic

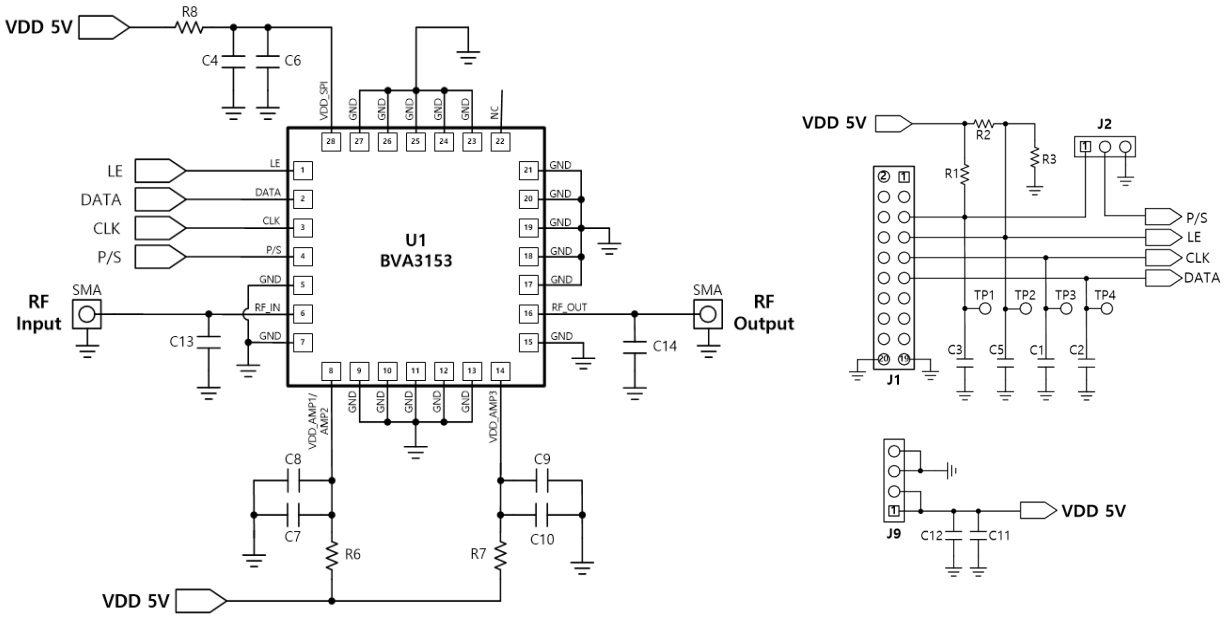
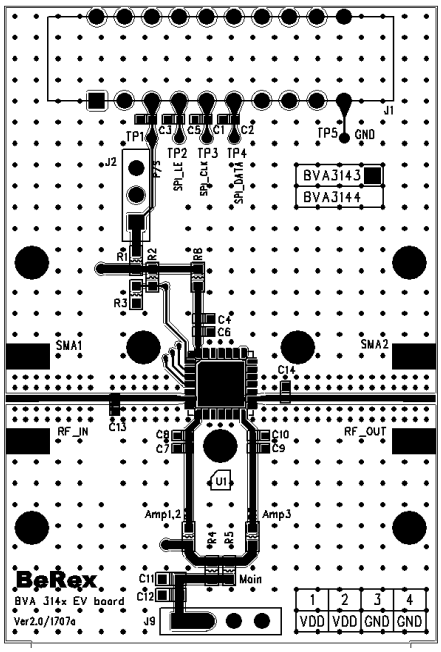


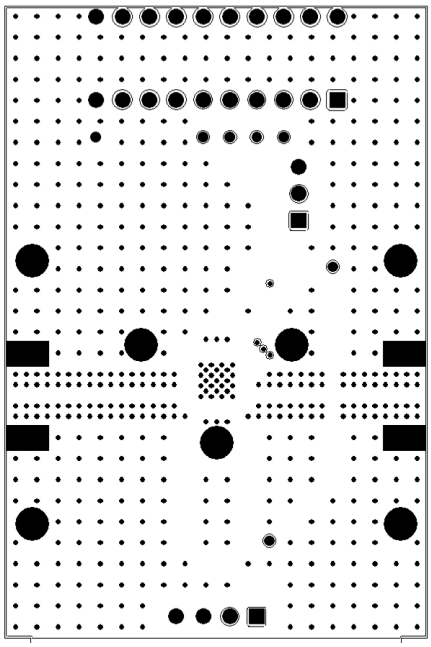
Table 10. Bill of material

No.	Ref. Number	Value	Description	Manufacturer
1	R2	100KΩ	Resistor, 0603, Chip, 5%	KOA Speer
2	R3	200KΩ	Resistor, 0603, Chip, 5%	KOA Speer
3	R6	0Ω	Jumper Resistor, 0603, Chip	KOA Speer
4	R7	0Ω	Jumper Resistor, 0603, Chip	KOA Speer
5	R8	0Ω	Jumper Resistor, 0603, Chip	KOA Speer
6	C4	100nF	Capacitor, 0402, Chip, 5%	Murata
7	C7	100nF	Capacitor, 0402, Chip, 5%	Murata
8	C10	100nF	Capacitor, 0402, Chip, 5%	Murata
9	C11	1uF	Capacitor, 0603, Chip, 5%	Murata
10	C12	1nF	Capacitor, 0603, Chip, 5%	Murata
11	C13	0.3pF	Capacitor, 0402, Chip, ±0.1pF	Murata
12	C14	0.7pF	Capacitor, 0402, Chip, ±0.1pF	Murata
13	SMA1	SMA	SMA(F) Connector, PCB Mount, PSF-S01-007	Gigalane
14	SAM2	SMA	SMA(F) Connector, PCB Mount, PSF-S01-007	Gigalane
15	J1	20pin	Receptacle Connector, 5-532955-3, Female,RT/A Dual	AMP Connectors
16	J2	3pin	2.54mm Breakaway Male Header, Straight, Black	
17	J9	4pin	2.54mm Breakaway Male Header, Straight, Black	
18	R1,C1,C2,C3,C5 C6, C8, C9	NC	Not connected	

Figure 34. Evaluation Board Layout



[Top View]



[Bottom View]

Figure 35. Evaluation Board PCB Layer Information

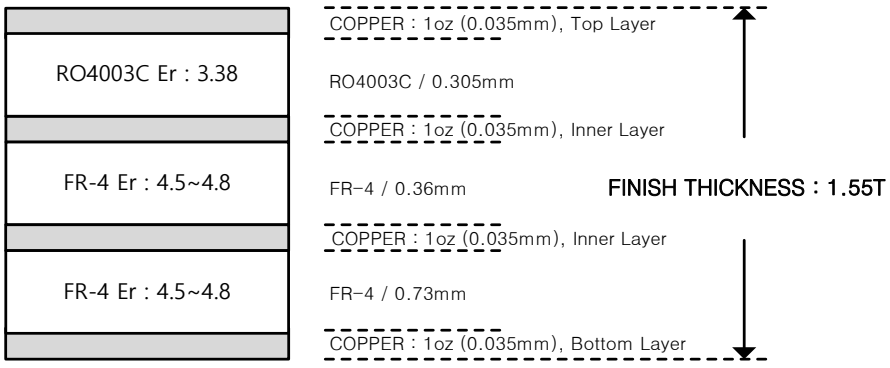


Figure 36. Suggested PCB Land Pattern and PAD Layout

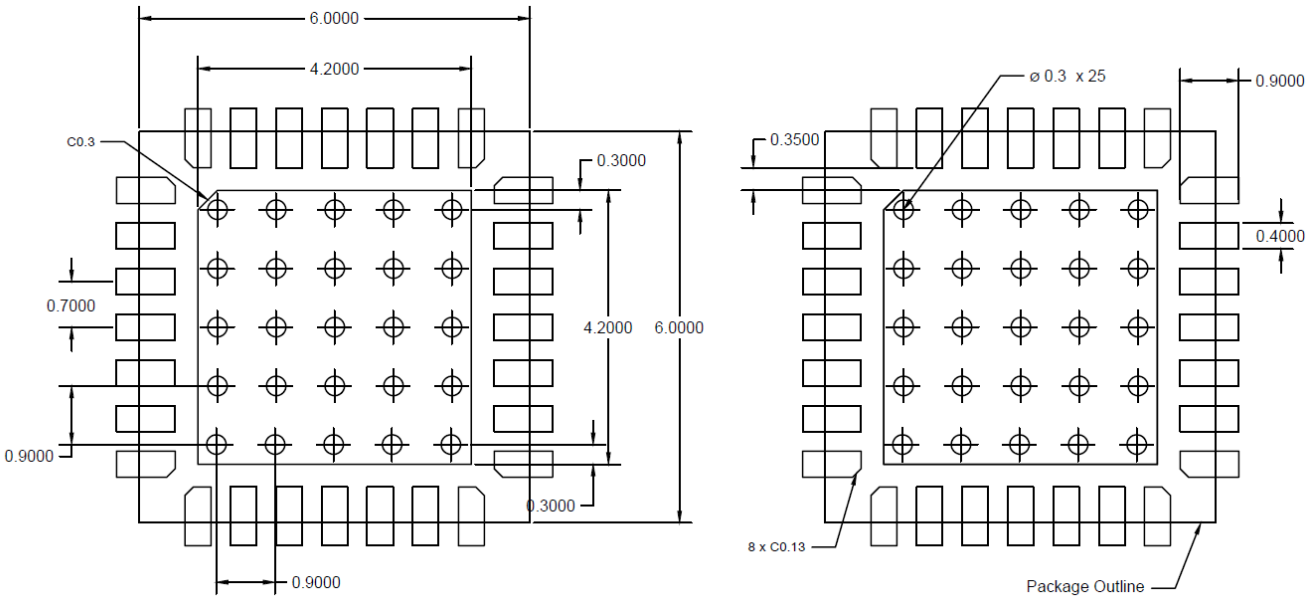
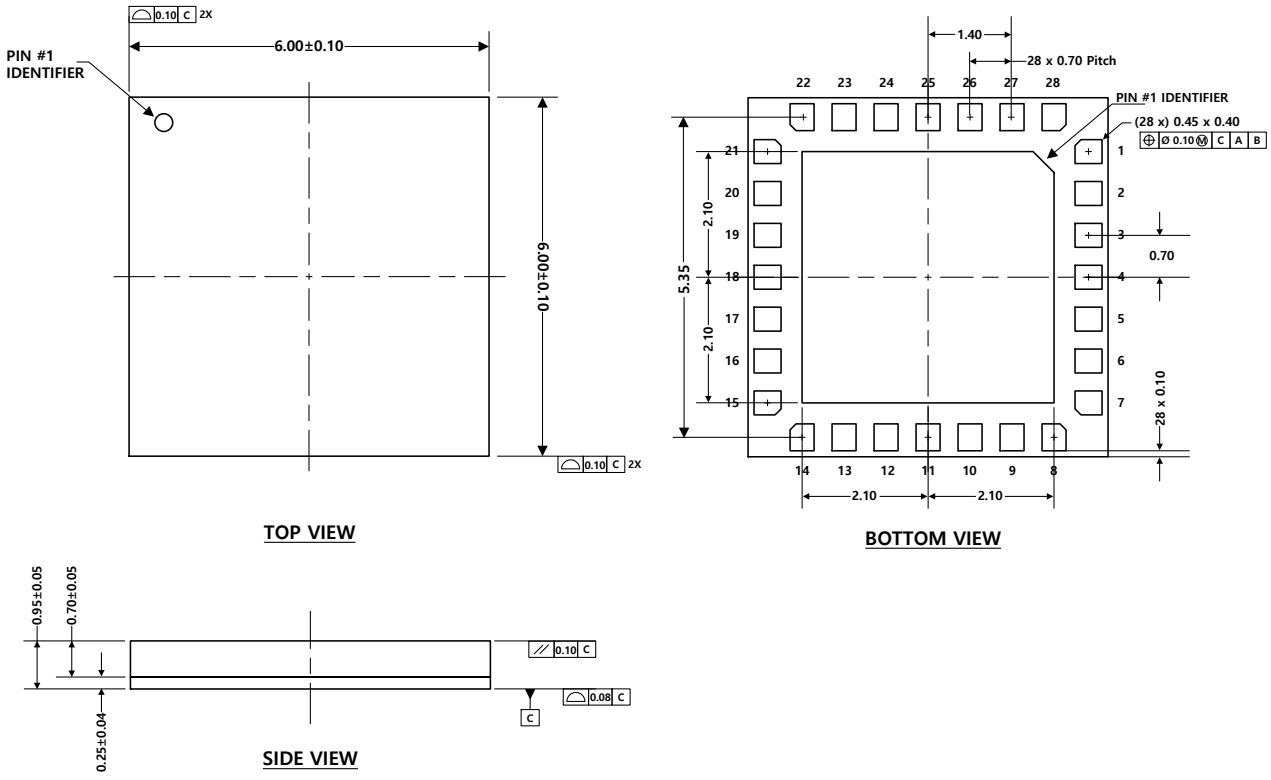


Figure 37. Packing Outline Dimension



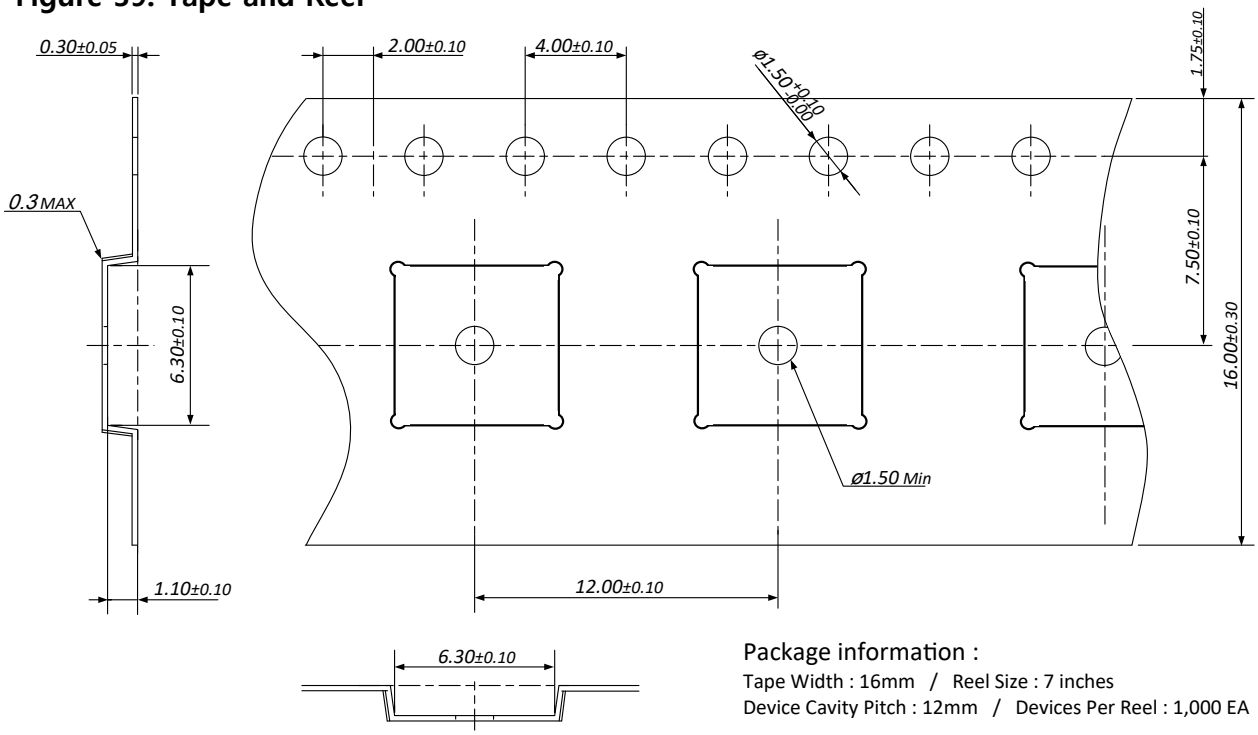
Notes

1. All dimensions are in millimeters. Angles are in degrees
2. Dimension and tolerancing conform to ASME Y14.5M-1994.

Figure 38. Package Marking Information

YY = Year
WW = Working Week
XX = Wafer Lot Number

Figure 39. Tape and Reel



Package information :

Tape Width : 16mm / Reel Size : 7 inches

Device Cavity Pitch : 12mm / Devices Per Reel : 1,000 EA

Lead Plating Finish

100% Tin Matte finish

(All BeRex products undergoes a 1 hour, 150 degree C, Anneal bake to eliminate thin whisker growth concerns.)

MSL / ESD Rating

ESD Rating :	Class 1C
Value :	1000V
Test :	Human Body Model (HBM)
Standard :	JEDEC Standard JS-001-2017

ESD Rating :	Class C5
Value :	1000V
Test :	Charged Device Model (CDM)
Standard :	JEDEC Standard JESD22-C101F

MSL Rating :	MSL3 at +260°C convection reflow
Standard :	JEDEC Standard J-STD-020

Caution : ESD Sensitive
Appropriate precautions in handling, packaging and testing devices must be observed.

Proper ESD procedures should be followed when handling the device.

RoHS Compliance

This part is compliant with Restrictions on the use of certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2011/65/EU as amended by Directive 2015/863/EU.

This product also is compliant with a concentration of the Substances of Very High Concern (SVHC) candidate list which are contained in a quantity of less than 0.1%(w/w) in each components of a product and/or its packaging placed on the European Community market by the BeRex and Suppliers.

NATO GAGE Code :

2	N	9	6	F