MegaChips

KL5BVCX400WMP

Video over Coax IC

Datasheet

Rev. 0.0.1

MegaChips

Revision History

Revision	Date	Description
0.0.1	2015/03/31	First draft

Table of Contents

1 Product overview

1.1 Function Overview

The KL5BVCX400WMP is a VOC (Video over Coax) device designed to simplify the connections of IP cameras to NVR (Network Video Recorders) and monitors. The chip can be used to extend the range between to the camera and NVR to over 2km using standard coax able. This enables fast and easy upgrades for analog camera systems as well new deployments of IP cameras that need longer distance than can be achieved with Ethernet cables.

The KL5BVCX400WMP supports up to 20 IP cameras on a single coax cable and a wide variety of topologies, as well as PoE (Power over Ethernet) and PoC (Power over Coax).

The KL5BVCX400WMP incorporates a 32-bit RISC processor and provides a single-chip implementation of high-performance wavelet conversion OFDM functionality, MAC processing functionality with high-quality QoS support, and VOC/Ethernet bridge functionality.

QoS functionality can be used to guarantee a fixed communication speed for a variety of communications ranging from data transmission and reception to video streaming and IP telephony.

The KL5BVCX400WMP also has highly integrated analog front-end chip so that no other analog front-end IC for VOC is necessary. An on-chip PLL multiplier and synthesizer provide all the required clock signals from a single crystal or clock source.

Following are the features of KL5BVCX400WMP.

- Single chip solution for VOC application.
- PoC support to send power over coax (40W @ 500M)
- Long Range
    - 45Mbps @2km RG6 cable
    - 30Mbps @2km RG59.
- 128-bit AES for secure communications
- Secure pairing capability
- Auto connect capability
- Easy network management and diagnostics
- Low Power 0.4W operating
- QoS support
- Industrial Temperature operation
- TQFP144 (18mm X18mm) package

1.2 Block Diagram

Figure- 1 shows a block diagram of the KL5BVCX400WMP.

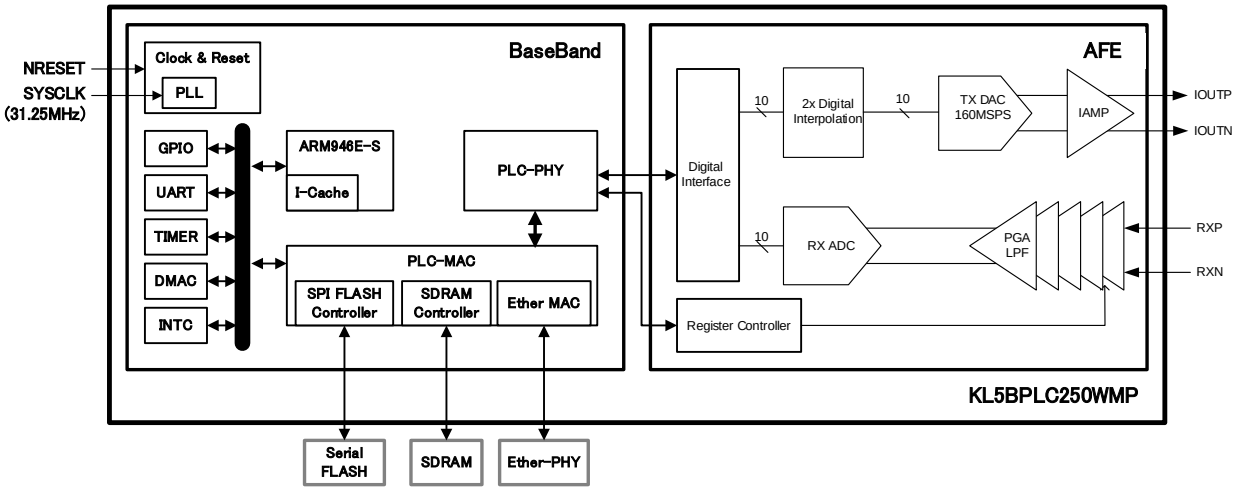


Figure- 1 KL5BVCX400WMP Block Diagram

2 Pins

2.1 Pin Assignments

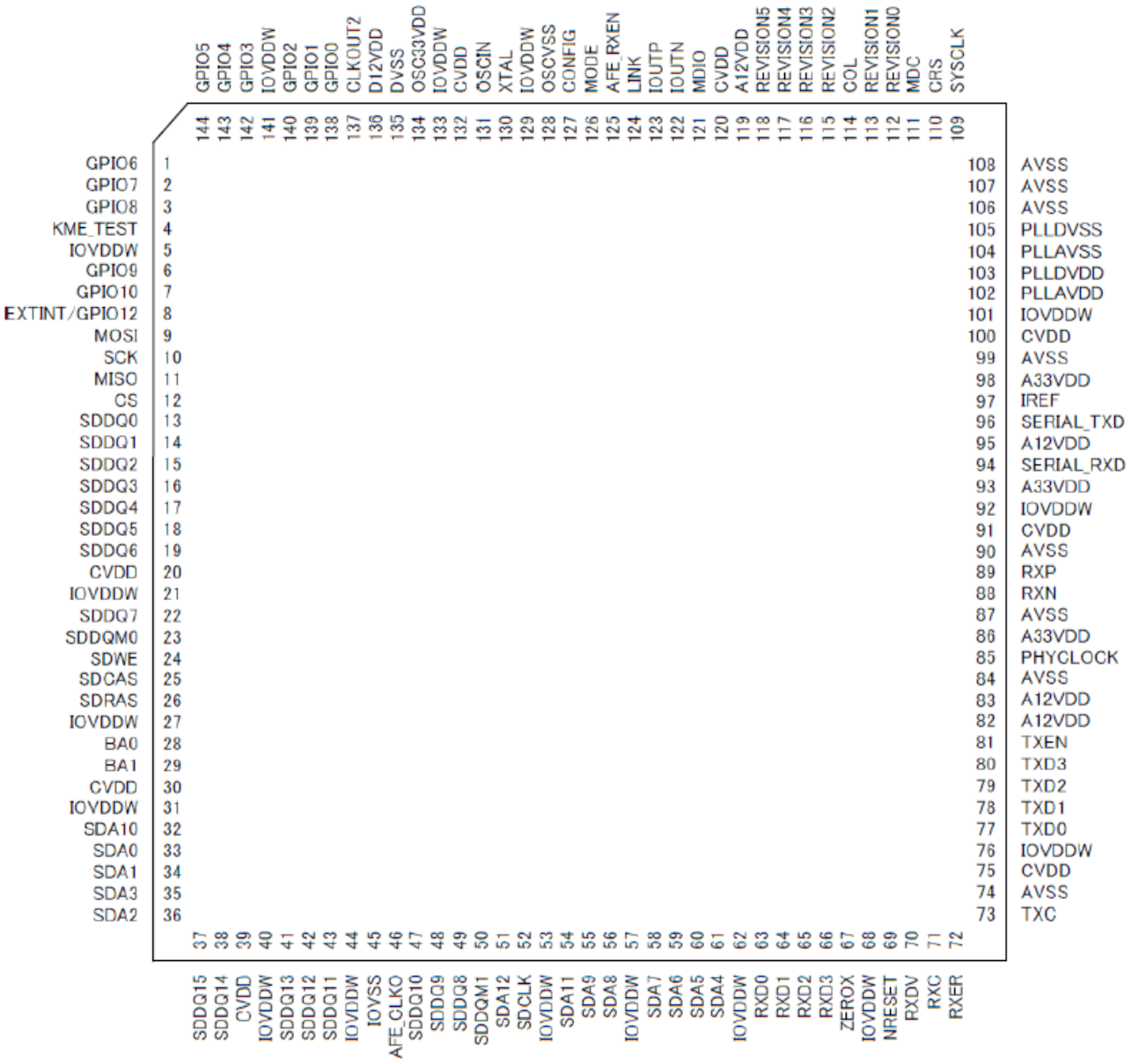


Figure- 2 Pin Assignment

2.2 Pin Descriptions

This section describes the KL5BVCX400WMP's pins. In the pin list, initial values for pins are given as “RST initial value”, and "---" means that initial values are undefined since those pins act as input in the initial state (following reset cancellation).

Pins whose names are followed by "(shared)" are treated as shared pins. Shared pins are not shown in Figure- 2.

2.2.1 Analog Front-end Connection Pins

Table- 1 shows a list of analog front-end connection pins.

Table- 1 List of Analog Front-end Connection Pins

No.	Pin Name	I/O	RST Initial Value	Pull-up/ Pull-down	Description
46	AFE_CLKO	O	Low	---	A/D / D/A sampling clock output.(62.5MHz)
125	AFE_RXEN	O	Low	Pull-down	Active high receive enable output.

2.2.2 Ethernet Connection Pins

The KL5BVCX400WMP's Ethernet connection pins comply with MII and RMII specifications and also support Turbo-MII specification. Register settings can be used to select the desired specification set.

Table- 2 shows a list of Ethernet connection pins.

Table- 2 List of Ethernet Connection Pins

No.	Pin Name	I/O	RST Initial Value	Pull-up/ Pull-down	Description
77	TXD0	O	Low	---	When MII/Turbo-MII is selected, act as 4-bit transmission data output. When RMII is selected, TXD0 and TXD1 act as 2-bit transmission data output pins. Do not connect anything to TXD2 or TXD3 in this configuration.
78	TXD1		Low	---	
79	TXD2		Low	---	
80	TXD3		Low	---	
81	TXEN	O	Low	---	Active high transmission data enable output.
73	TXC	I	---	---	Transmission clock input. Not used when RMII is selected. Requires pull-down.
63	RXD0	I	---	---	When MII/Turbo-MII is selected, act as 4-bit receive data input. When RMII is selected, RXD0 and RXD1 act as 2-bit receive data input. RXD2 and RXD3 act as monitor pins as described below: RXD2 : 10M/100M communications mode information RXD3 : LINK status
64	RXD1		---	---	
65	RXD2		---	---	
66	RXD3		---	---	
70	RXDV	I	---	---	Active high receive data valid input. When RMII is selected, connect to

					the EtherPHY SOC's CRS_DV pin.
71	RXC	I	---	---	Receive clock input Not used when RMII is selected. Requires pull-down.
72	RXER	I	---	---	Active high receive error indicator input.
114	COL	I	---	Pull-down	Active high collision detection input. Not used when RMII is selected. Requires pull-down.
110	CRS	I	---	Pull-down	Active high carrier sense input. Not used when RMII is selected. Requires pull-down.
121	MDIO	IO	---	Pull-down	Control data input/output.
111	MDC	O	Low	---	Control data clock output.
85	PHYCLOCK	O	Low	---	Acts as the Ethernet clock output. The clock precision is the same as for the clock input to the SYSCLK pin. When MII is selected, outputs 25MHz. When RMII, Turbo-MII are selected, outputs 50MHz.
124	LINK	I	---	Pull-up	Acts as the link state input. For more information about the pin level (indicating the presence of the link state), see the specifications for the EtherPHY SOC to which the pin will be connected. A toggle signal indicates that communications are in progress.

2.2.3 SDRAM Connection Pins

Table- 3 shows a list of SDRAM connection pins.

Table- 3 List of SDRAM Connection Pins

No.	Pin Name	I/O	RST Initial Value	Pull-up/ Pull-down	Description
13	SDDQ0	IO	---	---	16-bit data bus input/output for external SDRAM.
14	SDDQ1		---	---	
15	SDDQ2		---	---	
16	SDDQ3		---	---	
17	SDDQ4		---	---	
18	SDDQ5		---	---	
19	SDDQ6		---	---	
22	SDDQ7		---	---	
49	SDDQ8		---	---	
48	SDDQ9		---	---	
47	SDDQ10		---	---	
43	SDDQ11		---	---	
42	SDDQ12		---	---	
41	SDDQ13		---	---	
38	SDDQ14		---	---	
37	SDDQ15		---	---	
33	SDA0	O	Low	---	13-bit address bus output for external SDRAM.
34	SDA1		Low	---	
36	SDA2		Low	---	
35	SDA3		Low	---	
61	SDA4		Low	---	
60	SDA5		Low	---	
59	SDA6		Low	---	
58	SDA7		Low	---	
56	SDA8		Low	---	
55	SDA9		Low	---	
32	SDA10		Low	---	
54	SDA11		Low	---	
51	SDA12		Low	---	
28	BA0	O	Low	---	Bank address output for external SDRAM.
29	BA1		Low	---	
52	SDCLK	O	Low	---	SDRAM transfer clock output.
26	SDRAS	O	High	---	Bank select / row address strobe output.
25	SDCAS	O	High	---	Command select / column address strobe output.
24	SDWE	O	High	---	Write enable output.
23	SDDQM0	O	Low	---	Data mask control output.
50	SDDQM1	O	Low	---	

2.2.4 Serial Flash Connection Pins

Table- 4 shows a list of serial flash connection pins.

Table- 4 List of Serial Flash Connection Pins

No.	Pin Name	I/O	RST Initial Value	Pull-up/ Pull-down	Description
12	CS	O	High	---	Chip select output.
11	MISO	I	---	Pull-down	Serial data input.
10	SCK	O	Low	---	Serial clock output. (50MHz)
9	MOSI	O	Low	Pull-down	Serial data output

2.2.5 Serial Communication Connection Pins

Table- 5 shows a list of serial communication connection pins.

Table- 5 List of Serial Communication Connection Pins

No.	Pin Name	I/O	RST Initial Value	Pull-up/ Pull-down	Description
94	SERIAL_RXD	I	---	Pull-up	Serial data input.
96	SERIAL_TXD	O	Low	---	Serial data output.

2.2.6 General-purpose Ports

Table- 6 shows a list of general-purpose ports.

Table- 6 List of General-purpose ports

No.	Pin Name	I/O	RST Initial Value	Pull-up/ Pull-down	Description
138	GPIO0	IO	---	Pull-down	General-purpose port.
139	GPIO1	IO	---	Pull-down	General-purpose port.
140	GPIO2	IO	---	Pull-down	General-purpose port.
142	GPIO3	IO	---	Pull-down	General-purpose port.
143	GPIO4	IO	---	Pull-up	General-purpose port. (*1) Shared with AJTRSTN pin.
144	GPIO5	IO	---	Pull-up	General-purpose port. (*1) Shared with AJTDI pin.
1	GPIO6	IO	---	Pull-up	General-purpose port. (*1) Shared with AJTMS pin.
2	GPIO7	IO	---	Pull-up	General-purpose port. (*1) Shared with AJTCK pin.
3	GPIO8	IO	---	Pull-up	General-purpose port. (*1) Shared with AJRTCK pin.
6	GPIO9	IO	---	Pull-up	General-purpose port. (*1) Shared with AJTDO pin.
7	GPIO10	IO	---	Pull-up	General-purpose port. (*1) Shared with AJSRSTN pin.
8	GPIO12	IO	---	Pull-up	General-purpose port. (*2) Shared with EXTINT pin.

Note:

- *In normal mode, all ports are configured as input ports.*
- **1 : When ICE mode is selected, acts as the ICE JTAG pin.*
- **2 : Enabled by register settings.*
-

2.2.7 CPU Peripheral Connection Pin

Table- 7 shows a list of CPU peripheral connection pin.

Table- 7 List of CPU Peripheral Connection Pin

No.	Pin Name	I/O	RST Initial Value	Pull-up/ Pull-down	Description
8	EXTINT	I	---	Pull-up	Active Low external interrupt input. * Shared with GPIO12.

2.2.8 AC Synchronous Detection Pin

Table- 8 shows a list of AC synchronous detection pin.

Table- 8 List of AC Synchronous Detection Pin

No.	Pin Name	I/O	RST Initial Value	Pull-up/ Pull-down	Description
67	ZEROX	I	---	Pull-up	AC synchronous detection input.

2.2.9 Clock and Reset Pins

Table- 9 shows a list of clock and reset connection pins.

Table- 9 List of Clock and Reset Connection Pins

No.	Pin Name	I/O	RST Initial Value	Pull-up/ Pull-down	Description
109	SYSCLK	I	---	---	System clock input. (31.25MHz)
130	XTAL	O	---	---	Crystal Oscillator Inverter Output
131	OSCIN	I	---	---	Crystal Oscillator Inverter Input
137	CLKOUT2	O	---	---	f_{osc}/L Clock Output (L=1,2,4,8)
69	NRESET	I	---	Pull-up	Active low asynchronous reset input.

2.2.10 DAC Pins

Table- 10 shows a list of DAC connection pins.

Table- 10 List of DAC Connection Pins

No.	Pin Name	I/O	RST Initial Value	Pull-up/ Pull-down	Description
123	IOUTP	O	---	---	IAMP+ Current Output Sink
122	IOUTN	O	---	---	IAMP- Current Output Sink
97	IREF	I	---	---	Reference Current DAC, connect to 8.2kOhm resistor

2.2.11 ADC Pins

Table- 11 shows a list of ADC connection pins.

Table- 11 List of ADC Connection Pins

No.	Pin Name	I/O	RST Initial Value	Pull-up/ Pull-down	Description
89	RXP	I	---	---	Receive Path Analog Input pin
88	RXN	I	---	---	Receive Path Analog Input pin

2.2.12 Test Setting Pin

Table- 12 shows a list of test pins.

Table- 12 List of Test Setting Pin

No.	Pin Name	I/O	RST Initial Value	Pull-up/ Pull-down	Description
4	KME_TEST	I	---	Pull-down	Production test mode setting input. In normal operation, this input should be tied to low.
126	MODE	I	---	---	Vendor test purpose only, Fixed to “Low”
127	CONFIG	I	---	---	Vendor test purpose only, Fixed to “Low”

2.2.13 Debugger Connection Pins

Table- 13 shows a list of debugger connection pins.

Table- 13 List of Debugger Connection Pins

No.	Pin Name	I/O	RST Initial Value	Pull-up/ Pull-down	Description
143	AJTRSTN(Shared)	I	---	Pull-up	JTAG reset signal. * Shared with GPIO4.
144	AJTDI(Shared)	I	---	Pull-up	JTAG test data input. * Shared with GPIO5.
1	AJTMS(Shared)	I	---	Pull-up	JTAG TAP controller mode selection signal. * Shared with GPIO6.
2	AJTCK(Shared)	I	---	Pull-up	JTAG test clock. * Shared with GPIO7.
3	AJRTCK(Shared)	O	Low	Pull-up	JTAG Return TCK output to ICE. * Shared with GPIO8.
6	AJTDO(Shared)	O	Hi-Z	Pull-up	JTAG test data output. * Shared with GPIO9.
7	AJSRSTN(Shared)	I	---	Pull-up	JTAG system reset signal. * Shared with GPIO10.

Note:

- *GPIO10 to GPIO4 cannot be used as general-purpose ports during ICE mode operation.*

2.2.14 Hardware Revision Setting Pins

Table- 14 shows a list of hardware revision setting pins. For more information, see Section 4.9.1 Special Pin Settings.

Table- 14 List of Hardware Revision Setting Pins

No.	Pin Name	I/O	RST Initial Value	Pull-up/ Pull-down	Description
112	REVISION0	I	---	---	Revision setting
113	REVISION1	I	---	---	Revision setting
115	REVISION2	I	---	---	Revision setting
116	REVISION3	I	---	---	Revision setting
117	REVISION4	I	---	---	Used as ICEMODE setting pin
118	REVISION5	I	---	---	Reserved. Fixed to “Low”

Note:

- *Always mount a pull-up resistor or pull-down resistor outside the chip for these pins.*

2.2.15 Power Supply and VSS Pins

Table- 15 shows a list of power supply and VSS pins.

Table- 15 List of Power Supply and VSS Pins

No.	Pin Name	Description
5,21,27,31,40,44,53,57,62,68,76,92, 101,129,133,141	IOVDDW	3.3-V I/O Buffer power supply pins
45	IOVSS	Digital I/O Buffer Ground for AFE chip
20,30,39,75,91,100,120,132	CVDD	1.2-V (core) power supply pins for BaseBand
136	D12VDD	1.2-V (core) power supply pins for AFE
135	DVSS	Digital Ground for AFE
86,93,98	A33VDD	3.3V Analog Power Supply pins for AFE
82,83,95,119	A12VDD	1.2V Analog Power Supply pins
74,84,87,90,99,106,107,108	AVSS	Analog Ground for AFE
102	PLLAVDD	1.2V Analog VDD pin for BaseBand PLL
104	PLLAVSS	Analog Ground pin for BaseBand PLL
103	PLLDVDD	1.2V Digital VDD pin for BaseBand PLL
105	PLLDVSS	Digital Ground for BaseBand PLL
134	OSC33VDD	Crystal Oscillator Buffer 3.3V Power Supply pin
128	OSCVSS	Crystal Oscillator Buffer Ground
Exposed Pad	VSS	Digital Ground

2.2.16 Shared Pins

Table- 16 shows a list of shared pins.

Table- 16 List of Shared Pins

No.	Pin Name	Shared Pin Name	Description
143	GPIO4	AJTRSTN	Switchable with normal mode/ICE mode settings.
144	GPIO5	AJTDI	Switchable with normal mode/ICE mode settings.
1	GPIO6	AJTMS	Switchable with normal mode/ICE mode settings.
2	GPIO7	AJTCK	Switchable with normal mode/ICE mode settings.
3	GPIO8	AJRTCK	Switchable with normal mode/ICE mode settings.
6	GPIO9	AJTDO	Switchable with normal mode/ICE mode settings.
7	GPIO10	AJSRSTN	Switchable with normal mode/ICE mode settings.
8	GPIO12	EXTINT	Can be switched with GPIO selection register settings.

3 Operating Conditions

3.1 Absolute Maximum Ratings

Table- 17 shows absolute maximum ratings.

Table- 17 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
External supply IO voltage	V_{IOVDDW}	-0.3 to 4.0	V
External supply Analog voltage	V_{A33VDD}	-0.3 to 4.0	V
External supply Analog voltage	$V_{OSC33VDD}$	-0.3 to 4.0	V
Internal supply voltage for BaseBand	V_{CVDD}	-0.3 to 1.32	V
Internal supply voltage for AFE (Analog Part)	V_{A12VDD}	-0.3 to 1.6	V
Internal supply voltage for AFE (Digital Part)	V_{D12VDD}	-0.3 to 1.6	V
Input pin voltage	V_I	-0.3 to V_{IOVDDW} +0.3	V
Analog Input/Output Voltage RXP,RXN,IREF IOUTP, IOUTN OSCIN, XTAL	 V_{A1} V_{A2} V_{A3}	 -0.3 to V_{A33VDD} +0.3 -0.3 to 6.0 -0.3 to $V_{OSC33VDD}$ +0.3	 V V V
Output current (2mA)	I_O	-5.2/+15.9	mA
Output current (4mA)	I_O	-10.6/+31.7	mA
Output current (8mA)	I_O	-21.2/+63.4	mA
Power dissipation	P_D	700	mW
Storage temperature	T_{stg}	-55 to 125	°C

Note:

- *The absolute maximum ratings are the limit values beyond which the IC may be damaged. Operation is not guaranteed under these conditions.*
- *Directly connect all VDD pins to external power supplies and ground all VSS pins.*
- *Ensure that the junction temperature (Tj) is 125°C or less during use.*

3.2 Recommended Operating Conditions

Table- 18 shows recommended operating conditions.

Table- 18 Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
External supply voltage	V_{IOVDDW} V_{A33VDD} $V_{OSC33VDD}$	---	3.1	3.3	3.5	V
Internal supply voltage	V_{CVDD} V_{A12VDD} V_{D12VDD}	---	1.1	1.2	1.3	V
Operating package surface temperature	T_C	Tj = 125°C	-40	---	85	°C

4 BaseBand Part

4.1 Block Diagram

Figure- 3 provides a block diagram for the KL5BVCX400WMP BaseBand part.

Figure- 3 KL5BVCX400WMP Block Diagram

4.2 List of Functions

4.2.1 Microcontroller and Peripherals

- CPU — ARM946E-S with 16 Kbyte Instruction Cache
- System Clock — 125MHz
- Interrupt Controller
- 16bit Timer — 8Channels
- Serial Communication Controller — 1Channel
- GPIO
- DMAC
- Debug Function — Embedded ICE

4.2.2 VOC-PHY Function

- Frequency bandwidth — 2 MHz to 28 MHz
- Transmission scheme — Wavelet OFDM
- Sampling frequency — 62.5 MHz
- Sub carrier — 360 carriers (without notch filter: 432 carriers) including flexible notch function
- Primary modulation scheme — 32-PAM to 2-PAM
- Transmission speed — 240Mbps
- Error correction schemes — LDPC-CC, Reed-Solomon encoding and decoding / convolutional encoding +Viterbi decoding

4.2.3 VOC-MAC Processing Function

- Multiple access control method — CSMA/CA
- Data encryption functionality — 128bit AES
- Channel estimation control functionality
- Integrated IEEE 802.3 compliant MAC
- Integrated SDRAM controller

4.2.4 SPI FLASH Interface Function

- SPI (Serial Peripheral Interface) — Flash memory control functionality
- Clock frequency — 50MHz
- Boot RAM — 4Kbyte integrated boot RAM

4.2.5 SDRAM Interface Functions

- Clock frequency — 125MHz
- Data bus width — 16-bit
- Support Capacity — 16MByte/32MByte
- Row Address — 12-bit(16MByte Device)/13-bit(32MByte Device)
- Column Address — 8-bit/9-bit(16MByte, 32MByte Device) (8MBytes device is unsupported)

4.2.6 Ethernet PHY Interface Functions

- Supported interface — MII/RMII/Turbo-MII
- Clock frequency — 25MHz(MII)/50MHz(RMII, Turbo-MII)

4.2.7 Clock and Reset Control Functions

- Clock generation — 25MHz / 31.25MHz / 50MHz / 62.5MHz / 125MHz / 250MHz
- Reset control functionality
- Low-power mode control functionality — Link signal monitoring function

4.3 Example System Architectures

This section illustrates example normal mode and ICE mode system architectures for the KL5BVCX400WMP. For more information about these modes, see Section 4.6.1 Normal and Test Modes.

4.3.1 Normal Mode

Figure- 4 illustrates an example of normal mode system architecture.

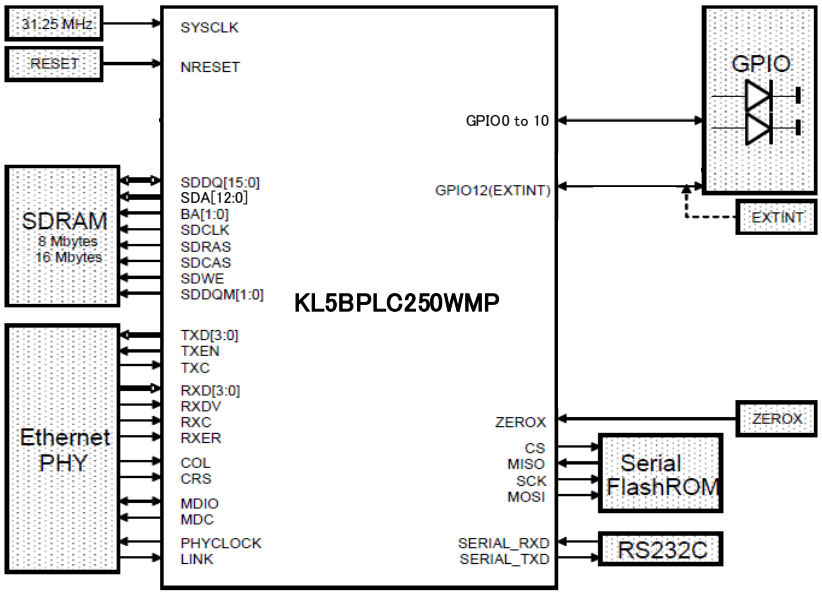


Figure- 4 Normal Mode Connection Diagram

4.3.2 ICE Mode

Figure- 5 illustrates an example of ICE mode system architecture.

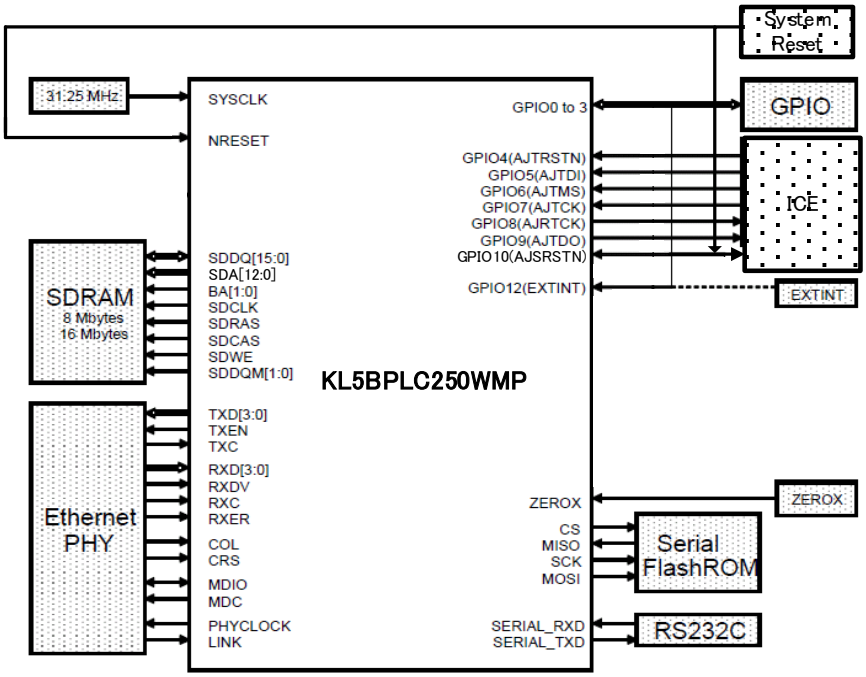


Figure- 5 ICE Mode Connection Diagram

Note:

- *GPIO10 to GPIO4 cannot be used as general-purpose ports during ICE mode operation.*
- *The rest of GPIO can be used as GPO, but not as GPI.*
  After reset, GPIO is set to the input, and turn into the output immediately.
  **GPIO12's EXTINT function is available even during ICE mode operation.*

4.4 Electrical Characteristics

Table- 19 show electrical characteristics.

Table- 19 Electrical characteristics

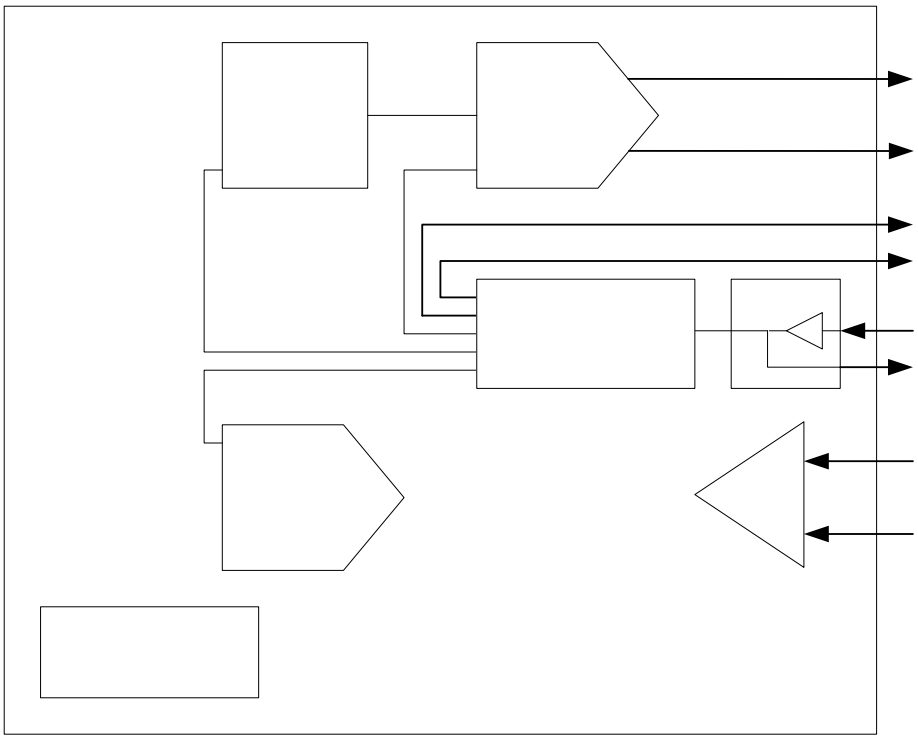
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input high voltage	V_{IH}	---	2.0	---	5.5	V
Input low voltage	V_{IL}	---	-0.3	---	0.8	V
Input threshold voltage	V_T	---	1.30	1.40	1.50	V
Schmitt Trigger Input threshold voltage	V_{T+}	Low to High	1.56	1.68	1.77	V
	V_{T-}	High to Low	1.14	1.23	1.33	V
Input leakage current	I_{LI}	$V_I = V_{IOVDDW}$ or V_{SS}	---	---	±10	μA
Pull-up resistor	R_{IH}	$V_I = V_{SS}$	26	38	59	kΩ
Pull-down resistor	R_{IL}	$VI = V_{IOVDDW}$ or V_{SS}	33	47	81	kΩ
Output high voltage	V_{OH}	---	2.4	---	---	V
Output low voltage	V_{OL}	---	---	---	0.4	V
Output leakage current	O_{LI}	$V_I = V_{IOVDDW}$ or V_{SS} $V_O = V_{IOVDDW}$ or V_{SS}	---	---	±10	μA

Conditions: V_{IOVDDW} = 3.3 V ± 0.3 V, V_{CVDD} = 1.2 V ± 0.12 V, -40°C < Tj < 125°C

5 Analog Front-End(AFE) Part

5.1 General Description

The KL5BVCX400WMP has highly integrated analog front-end part for VoC. Data rate is supported up to 80 MSPS and 160 MSPS in Rx path and Tx path, respectively. Interfacing can be either binary or twos compliment, LSB or MSB first. A serial peripheral interface (SPI) allows software programmability of the front-end. An on-chip PLL multiplier and synthesizer provide all the required clock signals from a single crystal or clock source.



5.2.1 Power Supply Specifications

Table- 20 Power Supply Specifications

Parameter	Temp	Min	Typ	Max	Unit
SUPPLY VOLTAGES					
A12VDD, D12VDD	Full	1.1	1.2	1.3	V
A33VDD , IOVDDW, OSC33VDD	Full	3.1	3.3	3.5	V
POWER CONSUMPTION (HALF-DUPLEX) (f_{DATA} = 80 MSPS)					
Tx Mode					
I_{A12VDD} + I_{D12VDD} (1.2V Supply Current)	25°C		39		mA
I_{A33VDD} + $I_{IO33VDD}$ + $I_{OSC33VDD}$ (3.3V Supply Current)	25°C		37		mA
Rx Mode					
I_{A12VDD} + I_{D12VDD} (1.2V Supply Current)	25°C		70		mA
I_{A33VDD} + $I_{IO33VDD}$ + $I_{OSC33VDD}$ (3.3V Supply Current)	25°C		57		mA
POWER CONSUMPTION OF FUNCTIONAL BLOCKS (f_{DATA} = 80 MSPS)					
RxPGA (3.3V)	25°C		35		mA
ADC (1.2V)	25°C		39		mA
TxDAC (3.3V)	25°C		4		mA
IAMP + 28 mA output (3.3V)	25°C		30		mA
Reference (1.2V)	25°C		1		mA
CLK PLL, Synthesizer and 1.2V Logic(Rx)	25°C		30		mA
MAXIMUM ALLOWABLE POWER DISSIPATION	Full			490	mW
STANDBY POWER CONSUMPTION					
I_{VDD_TOT} (Total Supply Current)	Full		10		mA
POWER DOWN DELAY (USING PWD PIN)					
RxPGA	25°C		100		ns
ADC	25°C		20		ns
TxDAC	25°C		20		ns
IAMP	25°C		20		ns
CLK PLL and Synthesizer	25°C		20		ns
POWER UP DELAY (USING PWD PIN)					
RxPGA	25°C		7		µs
ADC	25°C		5.5		µs
TxDAC	25°C		9	13	µs
IAMP	25°C			1	µs
CLK PLL and Synthesizer	25°C			410	µs
WAKE UP TIME (FROM SLEEP)					
RxPGA & ADC	Full			1	µs
DAC & IAMP (95% OUTPUT CURRENT)	Full			1	µs

O33VDD=OSC33VDD=A33VDD=3.3V ±0.2V, D12VDD=A12VDD=1.2V ± 0.1V
UNLESS OTHERWISE NOTED

5.2.2 Digital Interface Specifications

Table- 21 Digital Interface Specifications

Parameter	Temp	Min	Typ	Max	Unit
CMOS LOGIC INPUTS					
High Level Input Voltage	Full	2.0			V
Low Level Input Voltage	Full			0.8	V
Input Leakage Current	Full			10	µA
Input Capacitance	Full		3		pF
CMOS LOGIC OUTPUTS (C_{LOAD} = 5 pF)					
High Level Output Voltage ($_{IOH}$ = 2 mA)	Full	2.4			V
Low Level Output Voltage (I_{OH} = 2 mA)	Full			0.4	V
Output Rise/Fall Time (C_{LOAD} = 16 pF)	Full		2.2/2.2		ns
Output Rise/Fall Time (C_{LOAD} = 5 pF)	Full		1.2/1.1		ns
RESET					
Minimum Low Pulse Width (Relative to f_{ADC})		1			Clock cycles

IO33VDD=OSC33VDD=A33VDD=3.3V ±0.2V, D12VDD=A12VDD=1.2V ± 0.1V
UNLESS OTHERWISE NOTED

6 Package

Figure- 24 shows the package outline of KL5BVCX400WMP (Exposed TQFP-144 pins).

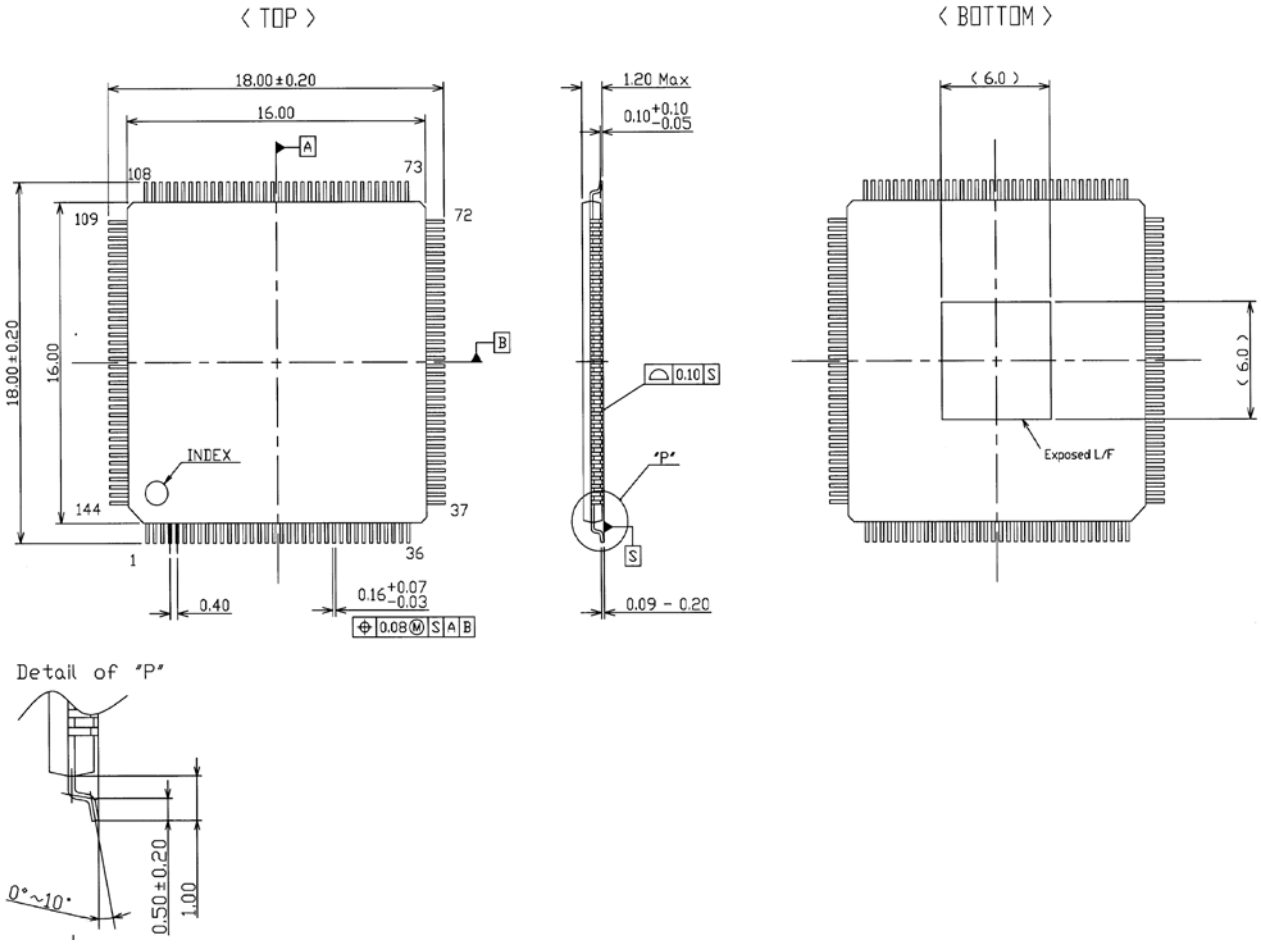


Figure- 7 KL5BVCX400WMP package outline (Exposed TQFP-144 pins)

7 Ordering Information

Part Number: KL5BVCX400WMP

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