GateMate™ FPGA Evaluation Board Datasheet

Evaluation Board Version 3.1

DS1003

Datasheet August 2022

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About this Document

This datasheet covers all features of the Cologne Chip GateMate™ FPGA evaluation board and is part of the GateMate™ documentation collection.

For more information please refer to the following documents:

- Technology Brief of GateMate™ FPGA
- **DS1001** – GateMate™ FPGA CCGM1A1 Datasheet
- **DS1002** – GateMate™ FPGA Programmer Board Ver. 1.3 Datasheet
- **UG1002** – GateMate™ FPGA Toolchain Installation User Guide

Cologne Chip provides a comprehensive technical support. Please visit our website for more information or contact our support team.

Revision History

This Datasheet is constantly updated. The latest version of the document can be found following the link below:

DS1003 – GateMate™ FPGA Evaluation Board Ver. 3.1 Datasheet

A brief description and download links can be found here:

GateMate™ FPGA Evaluation Board

Date	Remarks
August 2022	• Figure 3.2 (power supply unit) on page 22 added. • Table 3.8 (GPIO routing details) on page 35 added. • Bill of materials added in appendix C. • A few small fixes and improvements.
April 2022	Pmod signal assignment added (Table 3.9 on page 36).
March 2022	Initial release.

Chapter 1

Introduction

The GateMate™ FPGA Evaluation Board is a feature-rich, ready-to-use development platform for the CCGM1A1.

It serves as a reference design and for a direct entry into application development. It is the perfect starting point for all embedded designers as it features

- USB host access,
- JTAG interface,
- SPI interface,
- on-board flash memory,
- Serializer / Deserializer (SerDes) interface,
- Pmod-compatible interface,
- on-board HyperRAM module,
- 108 accessible general purpose input / outputs (GPIOs),
- 7 status LEDs.

The evaluation kit is available from Cologne Chip. Please visit our website for more information.

Figure 1.1 gives a brief overview of the evaluation board features. Some GPIO banks have fixed power level according to their function. Others can be configured to different voltages due to the user application requirements.

The printed circuit board (PCB) top view is shown in Figure 1.2. Please note, that some components are prepared for extended features and must be populated by the user, if needed.

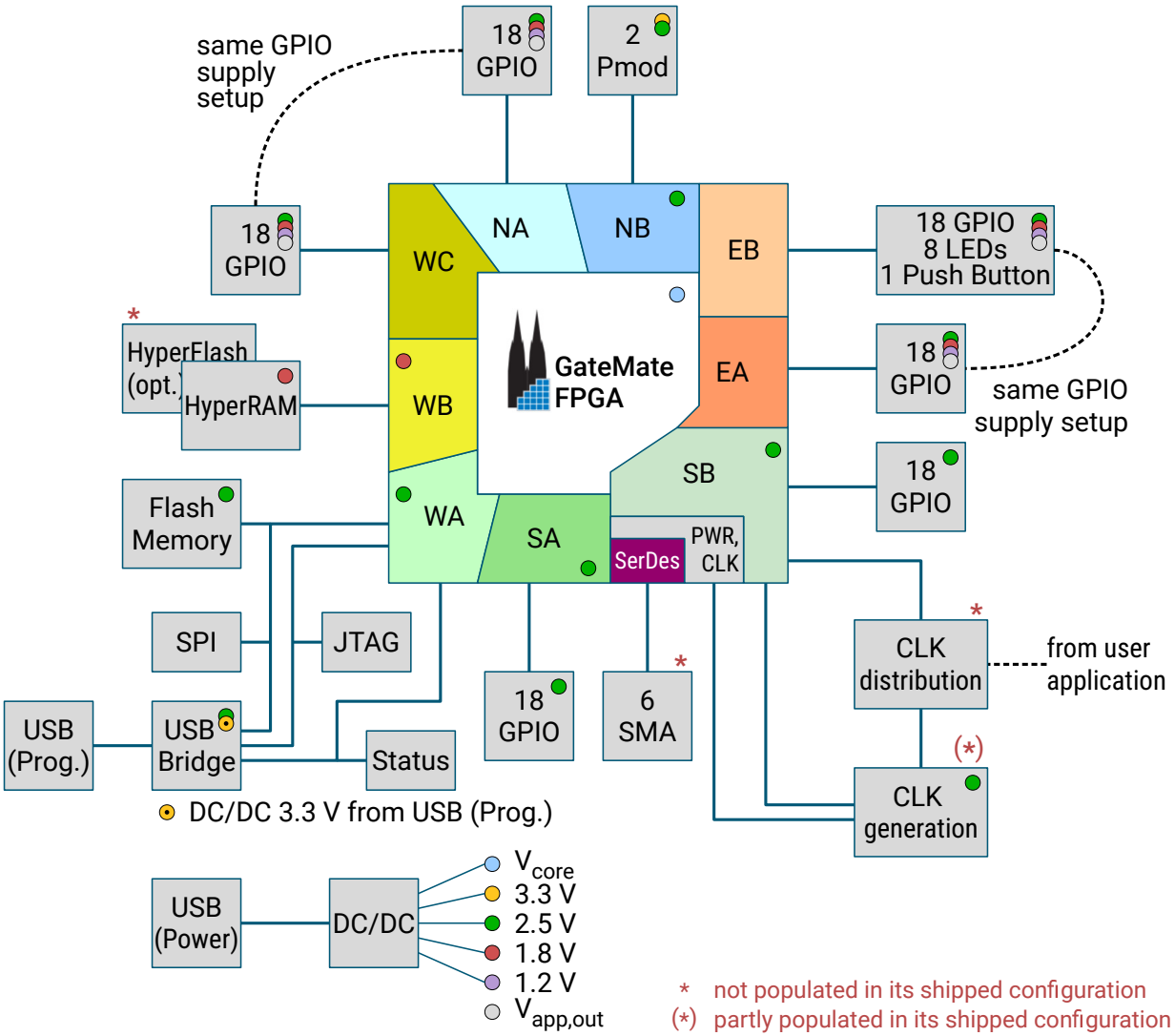


Figure 1.1: *Feature overview of the GateMate™ FPGA evaluation board version 3.1*

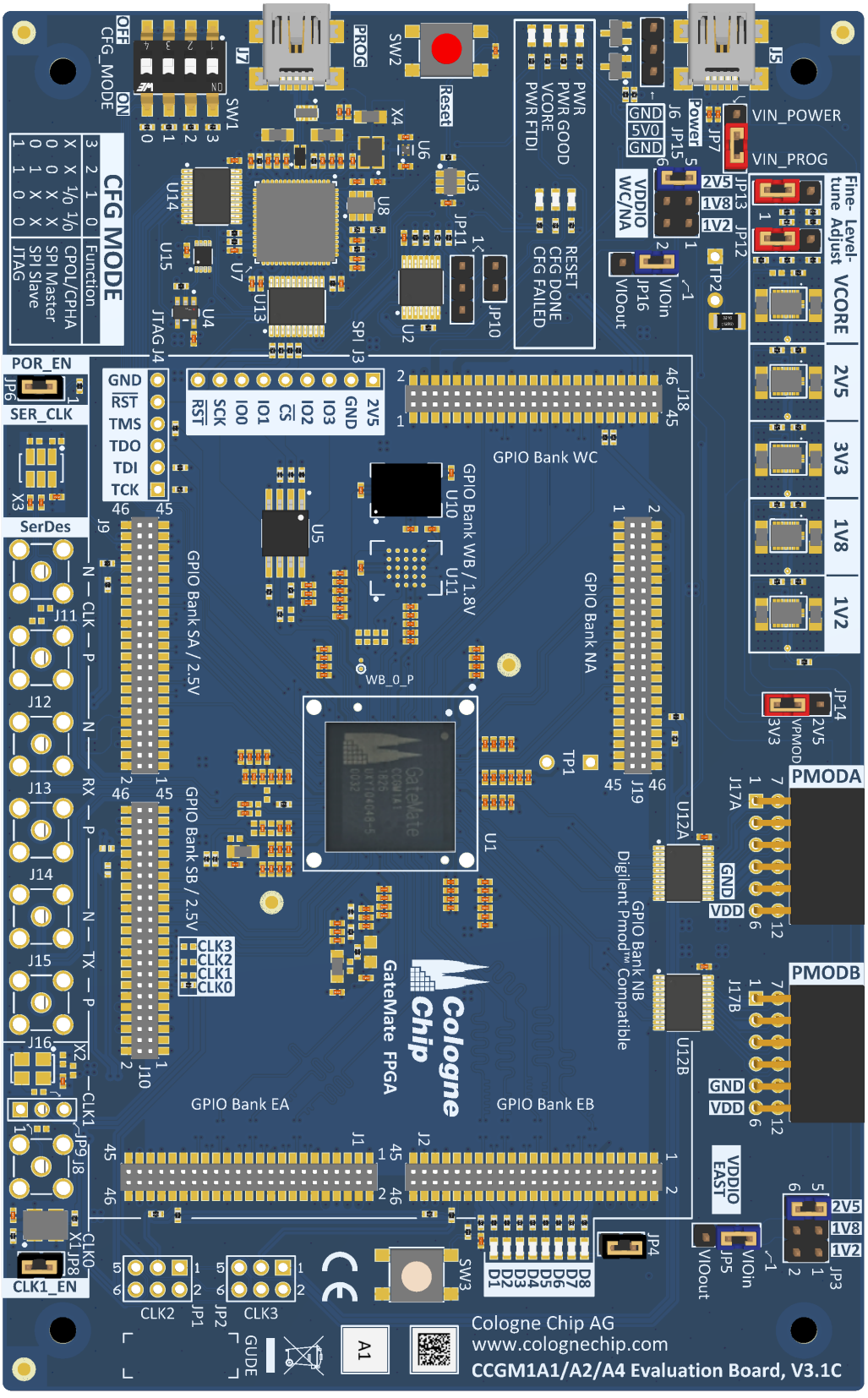


Figure 1.2: *GateMate™ FPGA evaluation board version 3.1*

Chapter 2

Startup

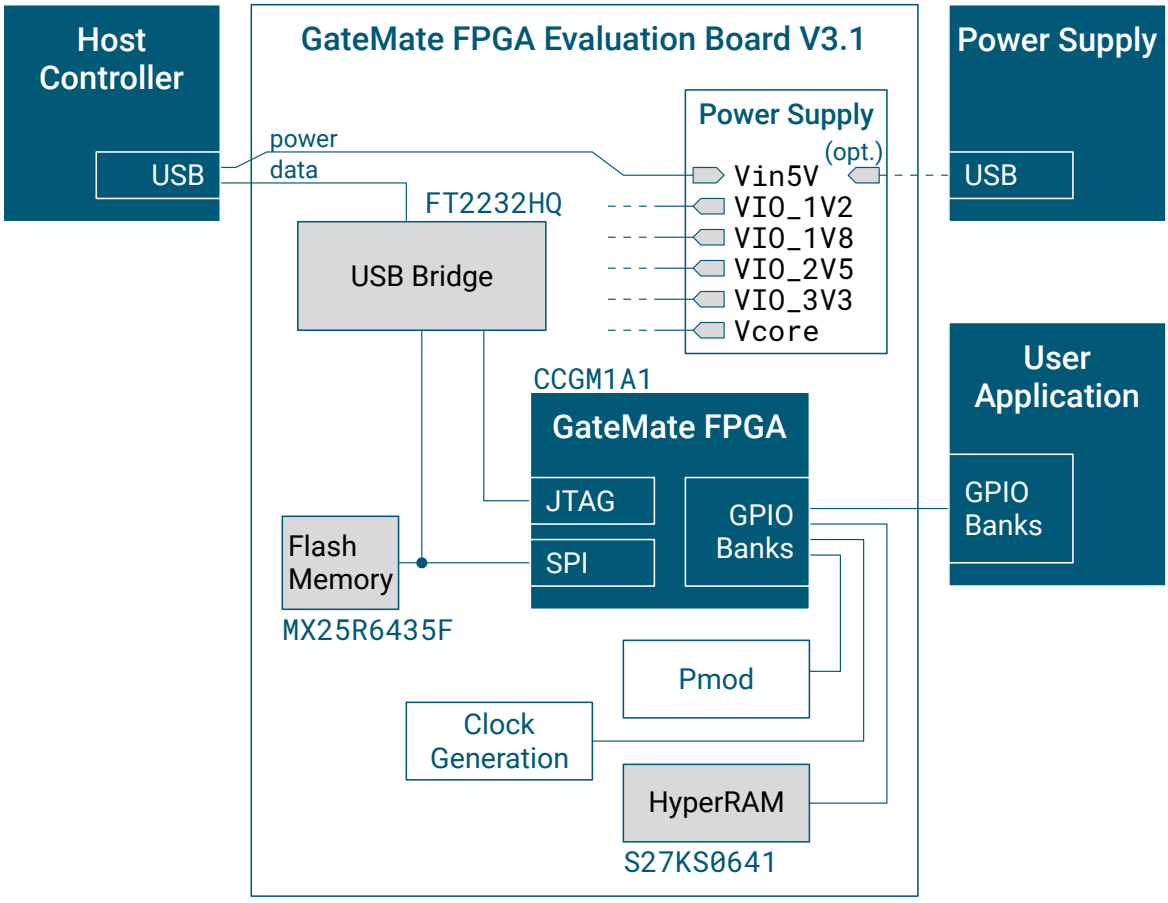


Figure 2.1: *Block diagram of the GateMate™ FPGA evaluation board*

2.1 Block Diagram

The GateMate™ FPGA evaluation board offers a quick access to the CCGM1A1 functions. Figure 2.1 gives a simplified overview of the printed circuit board (PCB) block diagram. A single supply voltage from any USB supply is typically used for powering the PCB and the user application.

The FPGA configuration can be loaded in two different ways. The on-board flash memory can automatically set up the FPGA configuration after reset. Alternatively, a host controller can be used to load the FPGA configuration. These functions and additional features on the SPI und JTAG interface are described in Chapter 3.3 from page 27.

The user application connects the general purpose input / output (GPIO) banks of the GateMate™ FPGA and some additional signals like reset and clock to fulfill further application requirements.

2.2 Connection to the User Application

The interface to the GPIO banks is implemented with 2-row 46-pin through-hole connectors with pin pitch 1.27 mm. The user application can use standard male pin header 2×23 to connect the GPIO banks and some further signals.

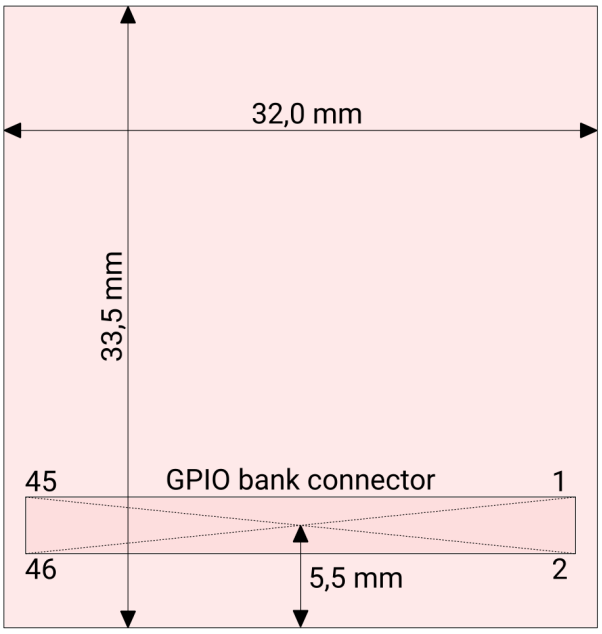


Figure 2.2: *Recommended maximum dimensions of a user application PCB for a single GPIO bank and horizontal assembly (top view)*

Due to through-hole technology, the user application can either be connected at the top side of the evaluation board, or it can be mounted below. It is usually advisable to assemble the user application on the top side for an easy access to the user circuitry. Then,

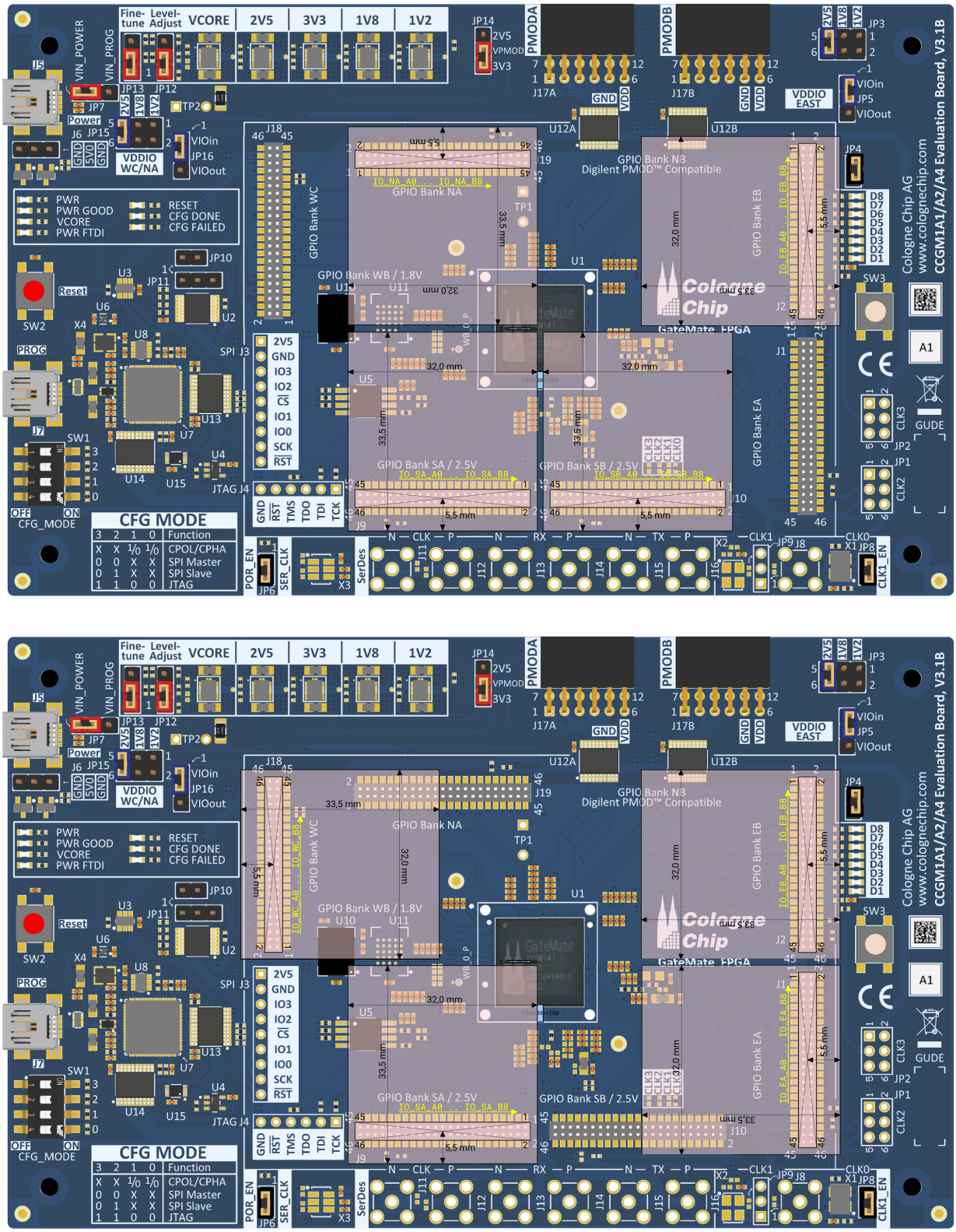


Figure 2.3: *Examples of assembling several 1-bank user applications at the same time*

it should be noted that all tall components are outside the rectangular area of the GPIO bank connectors.

For a user application with access to a single GPIO bank, e.g., the maximum PCB dimensions should not exceed 32.0×33.5 mm for horizontal assembly. Furthermore, the location of the GPIO pin header should be as shown in Figure 2.2. With this arrangement,

a) the user PCB can be plugged onto every GPIO bank and
b) several user PCBs can be used at the same time as shown in Figure 2.3.

When assembling the user PCB below the evaluation board there are no restrictions due to tall components.

When assembling the user PCB upright, there are no restrictions concerning the user PCB length. However, the specified width of 32.0 mm should not be exceeded.

For the design of user applications with more than one GPIO bank please see the evaluation board dimensions in Figure 5.1 on page 42.

2.3 Connection to the Host Controller

The GateMate™ FPGA Evaluation Board requires a computer with Linux or Windows operating system as follows:

- Supported Linux environments:
  - Debian-based Linux (Debian, Ubuntu, ...) with `apt` package manager
  - Arch-based Linux (Arch, Manjaro, ...) with `pacman` package manager
  - Red Hat-based Linux (Fedora, ...) with `dnf` or `yum` package manager
- Windows environments:
  - Windows 7 or later, 64 bit
  - Zadig USB driver installer (`https://zadig.akeo.ie/`)

When first plugged into the computer's USB port, drivers should load by default.

In Windows environments, it is necessary to install USB drivers using Zadig. Download the software and connect the GateMate™ Evaluation Board to your USB port. In the Zadig Window, select **Options > List All Devices** to refresh the device list. From the drop-down list, select **GateMate FPGA Evalboard 3.1B (Interface0)**. Now select **libusb-win32 (any version)** from the driver list and replace the drivers (see Figure 2.4).

Replacing drivers might take a moment. Repeat this procedure for interface 1. Your GateMate™ Evalution Board should then be listed as **libusb-win32 device**s in the Device Manager as shown in Figure 2.5.

In Linux environments, drivers are automatically loaded correctly.

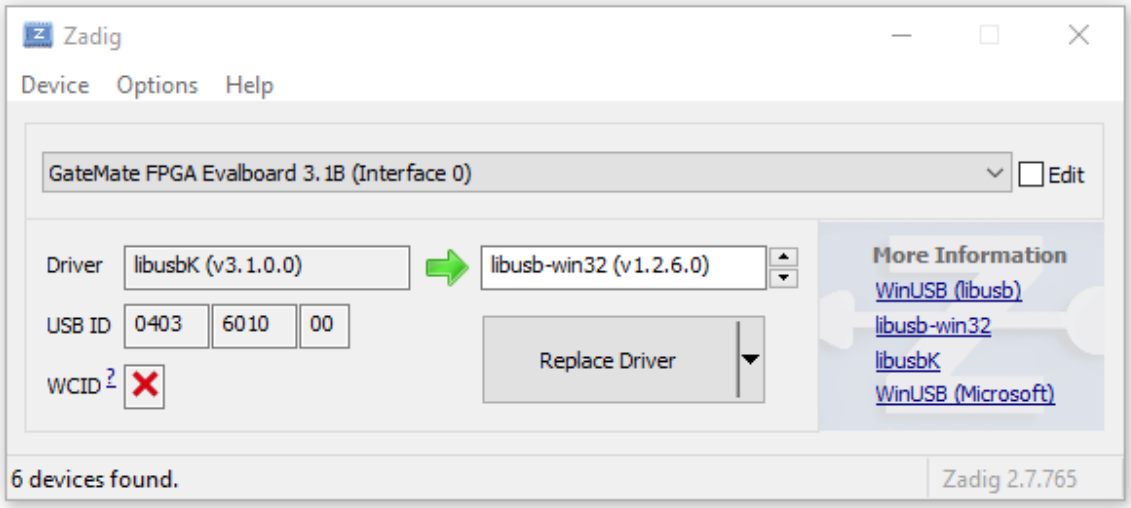


Figure 2.4: *Zadig Window with selected GateMate™ FPGA Evaluation Board*

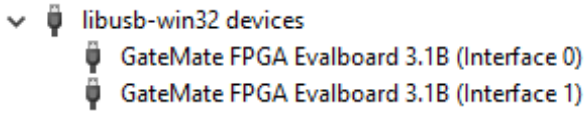


Figure 2.5: *GateMate™ FPGA Evaluation Board in Device Manager*

The tool setup for the Cologne Chip GateMate™ series is described in the user guide **UG1002** – GateMate™ FPGA Toolchain Installation User Guide

Chapter 3

GateMate™ FPGA Evaluation Board Functions

3.1 PCB Power Supply

The power supply unit consists of five DC-DC converters MPM3833C which offer all voltages to fulfill the requirements of a wide range of user applications. All converters are feed from a single source. Typically an USB supply can be used.

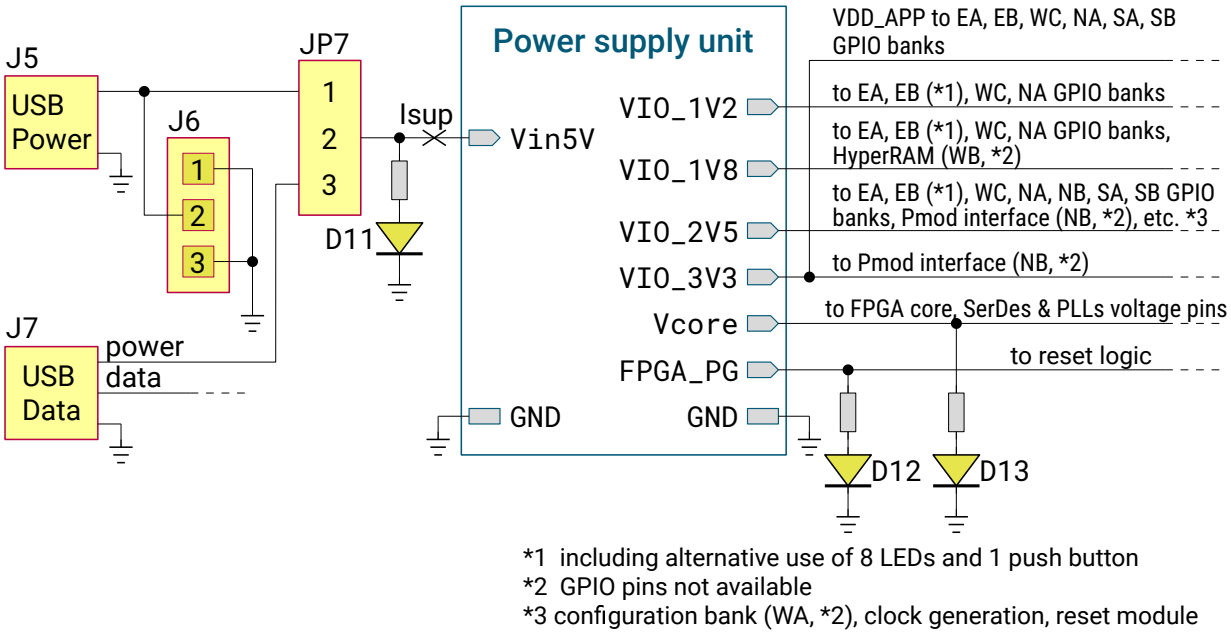


Figure 3.1: *PCB power supply*

Figure 3.1 shows that power supply can either be feed in from the USB connector J5 or it can be taken from the USB data connector J7 instead. Please ensure, that enough power can be delivered from the USB host.

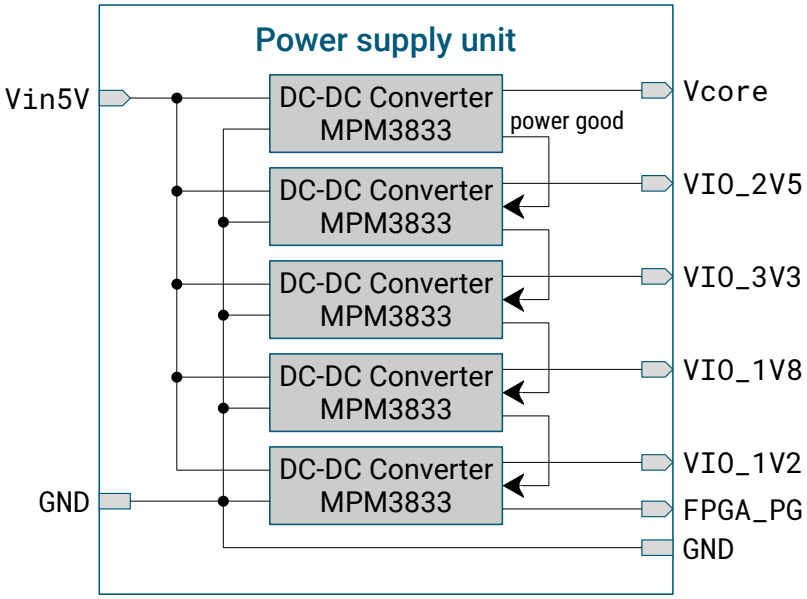


Figure 3.2: *DC-DC converter chain*

Alternatively, power supply can be feed from any other source via connector J6. The required input voltage is 4.0 . . 6.0 V.

All DC-DC converters are chained with their power good signal as shown in Figure 3.2. At the end of the chain, signal FPGA_PG is feed to the reset circuitry (see Figure 3.10 on page 30). The FPGA can only go into operation when all converters provide a stable output voltage.

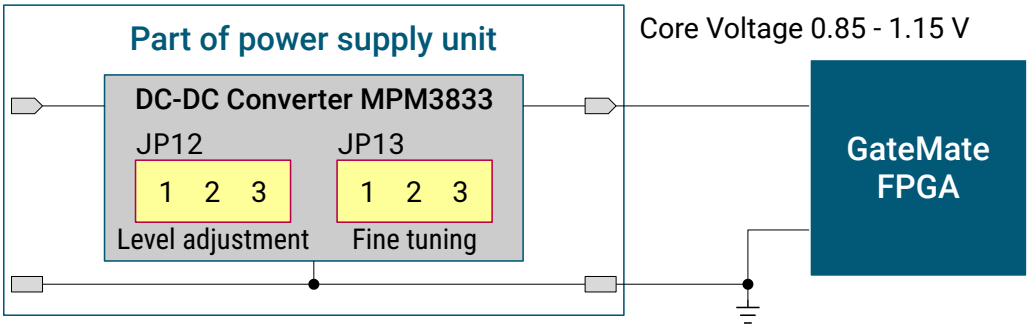


Figure 3.3: *GateMate™ FPGA core voltage*

The DC-DC converters have a fixed output voltage. Only the DC-DC converter for the FPGA core voltage can be adjusted as shown in the block diagram in Figure 3.3.

The FPGA core voltage can be set up to different levels for low power mode, economy mode or speed mode. Furthermore, typical voltage can be chosen as well as minimum and maximum levels. Jumper settings are described in Table 3.1.

Table 3.1: *JP12 and JP13 jumper settings for FPGA core voltage*

JP12	JP13	Core Voltage	Function
open	open	0.85 V	low power mode, min
open	1 - 2	0.90 V	low power mode, typical
open	2 - 3	0.95 V	low power mode, max
1 - 2	open	0.95 V	economy mode, min
1 - 2	1 - 2	1.00 V	economy mode, typical
1 - 2	2 - 3	1.05 V	economy mode, max
2 - 3	open	1.05 V	speed mode, min
2 - 3	1 - 2	1.10 V	speed mode, typical
2 - 3	2 - 3	1.15 V	speed mode, max

Important note:

Please ensure to disconnect the power supply before changing the jumper settings to avoid damage of the devices.

3.2 GPIO Power Supply

The CCGM1A1 FPGA offers nine general purpose input / output (GPIO) banks. Their GPIO supply voltage is set up in different ways on the evaluation board as shown in Table 3.2.

Table 3.2: *Assignment of GPIO power supply scheme to GPIO banks*

Figure	Page	GPIO banks	Scheme characteristics
3.4	24	WC, NA, EA	GPIO voltage selected from three on-board sources or the application voltage
3.5	25	EB	GPIO voltage selected from three on-board sources or the application voltage, additional functions (LEDs and user button)
3.6	26	SA, SB	Single 2.5 V voltage supply
–	–	WA	Configuration bank, 2.5 V supply
3.17	37	WB	HyperBus memory, 1.8 V supply
3.16	36	NB	Pmod interface, 2.5 V supply

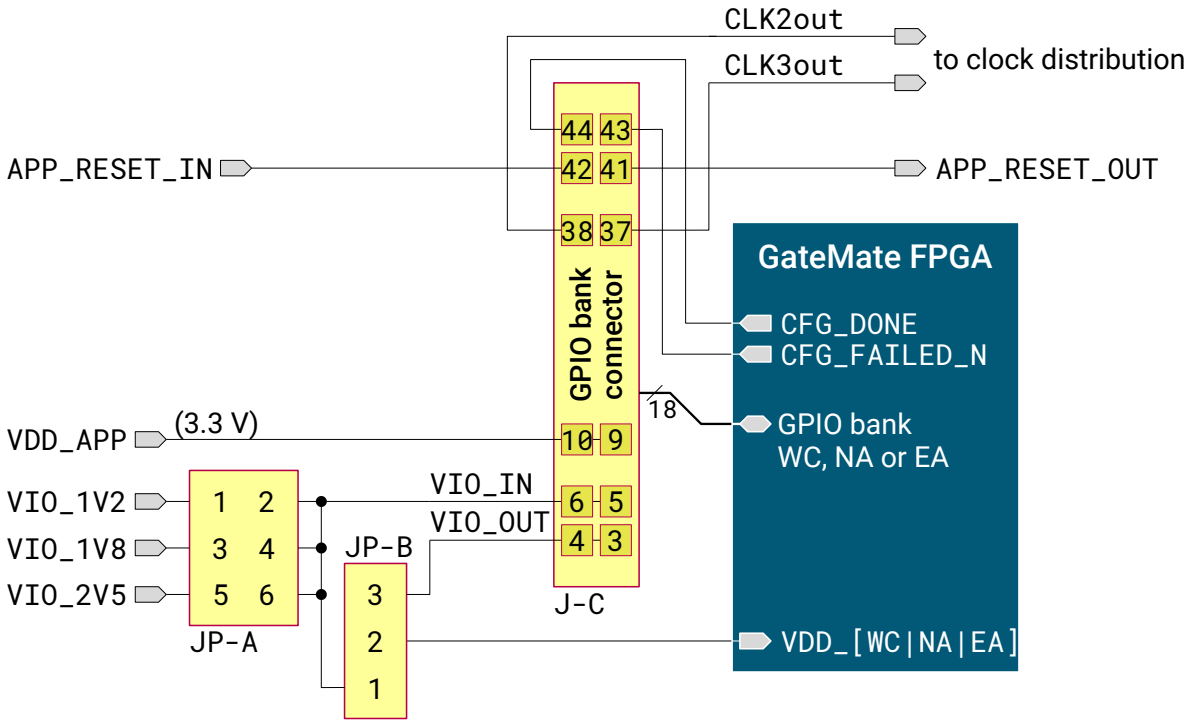


Figure 3.4: *GPIO supply with voltage selection*

Figure 3.4 shows the configurable GPIO supply setup for GPIO banks `WC`, `NA` and `EA`. These banks can select one of three on-board voltages as well as `VIO_OUT` feed from the user application. The selected on-board voltage is also feed to the user application (`VIO_IN`) and can be used to supplement the separat `VDD_APP` voltage.

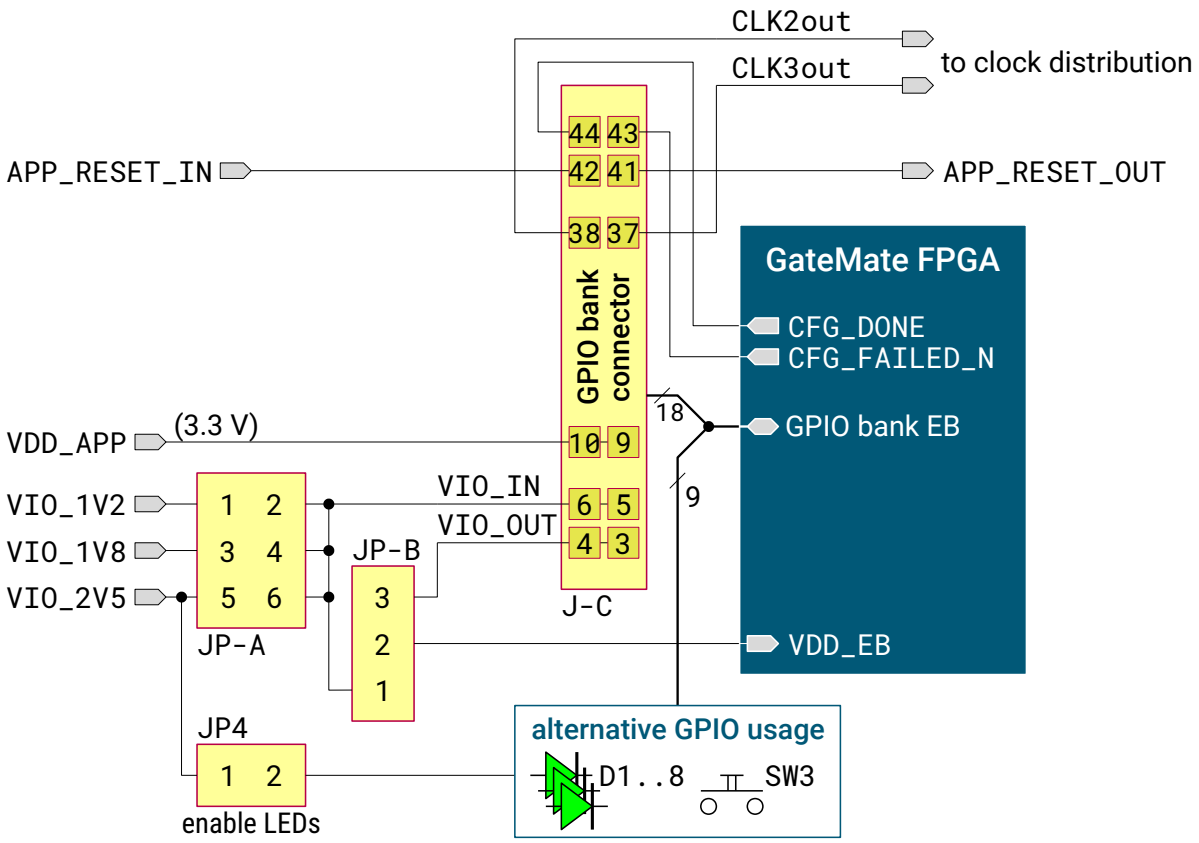


Figure 3.5: *GPIO supply with voltage selection and alternative LEDs and push button*

The same GPIO supply scheme is available for GPIO bank EB but additional functionality is implemented for some GPIO signals as shown in Figure 3.5 and Table 3.3. Eight LEDs can be enabled with Jumper JP4 set. With open jumper, the normal GPIO function is available at connector J-C (J2). Switch SW3 has an on-board pull-up resistor, which should be

Table 3.3: *Additional functions on GPIO bank EB*

Component	GPIO	Funktion
D1	IO_EB_B1	low: on (green), high: off
D2	IO_EB_B2	ditto
D3	IO_EB_B3	ditto
D4	IO_EB_B4	ditto
D5	IO_EB_B5	ditto
D6	IO_EB_B6	ditto
D7	IO_EB_B7	ditto
D8	IO_EB_B8	ditto
SW3	IO_EB_B0	pressed: low, unpressed: high

Table 3.4: *Jumper JP-A, JP-B and connector J-C designators*

Figure	JP-A	JP-B	J-C	GPIO bank
3.4 (page 24)	JP15	JP16	J18	WC
	JP15	JP16	J19	NA
	JP3	JP5	J1	EA
3.5 (page 25)	JP3	JP5	J2	EB
3.6 (page 26)	–	–	J9	SA
	–	–	J10	SB

taken into account when using the normal GPIO function instead. Table 3.3 shows the additional EB GPIO functions in detail.

Table 3.4 gives an overview of jumpers JP-A and JP-B and connector J-C availability for the individual GPIO banks.

Finally, GPIO banks SA and SB have a fixed supply voltage 2.5 V (see Figure 3.6). Again, the user application supply is both, VDD_APP and the GPIO voltage VIO_2V5.

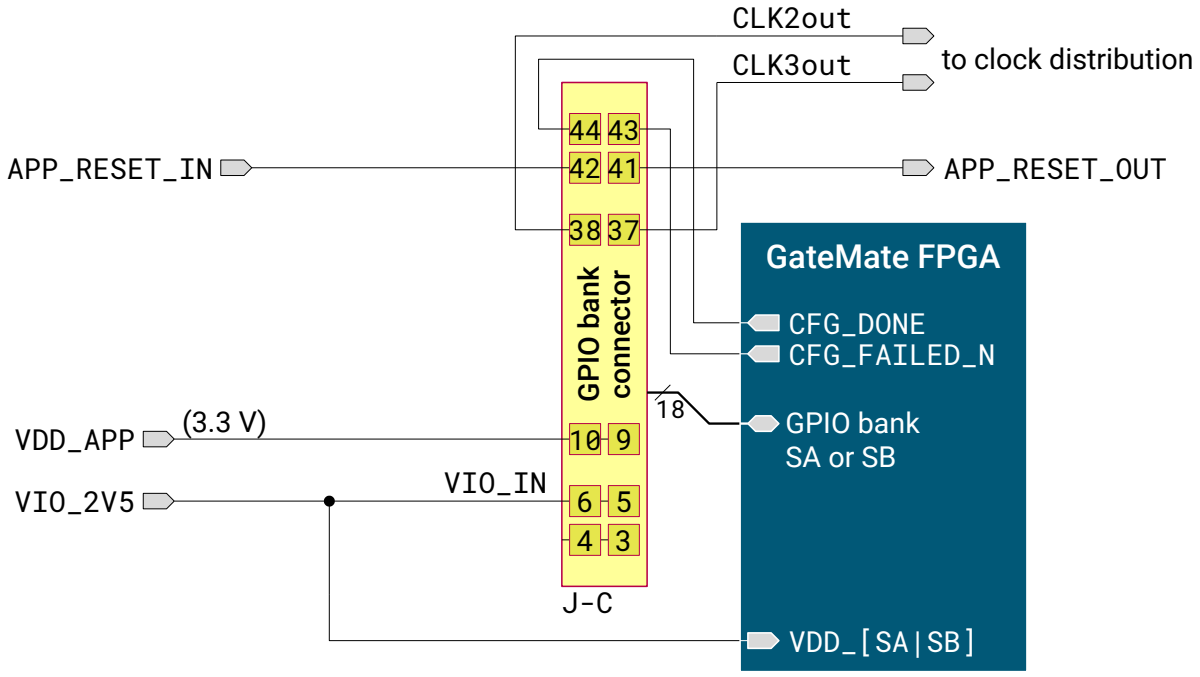


Figure 3.6: *GPIO supply with single voltage*

3.3 SPI and JTAG Data Busses

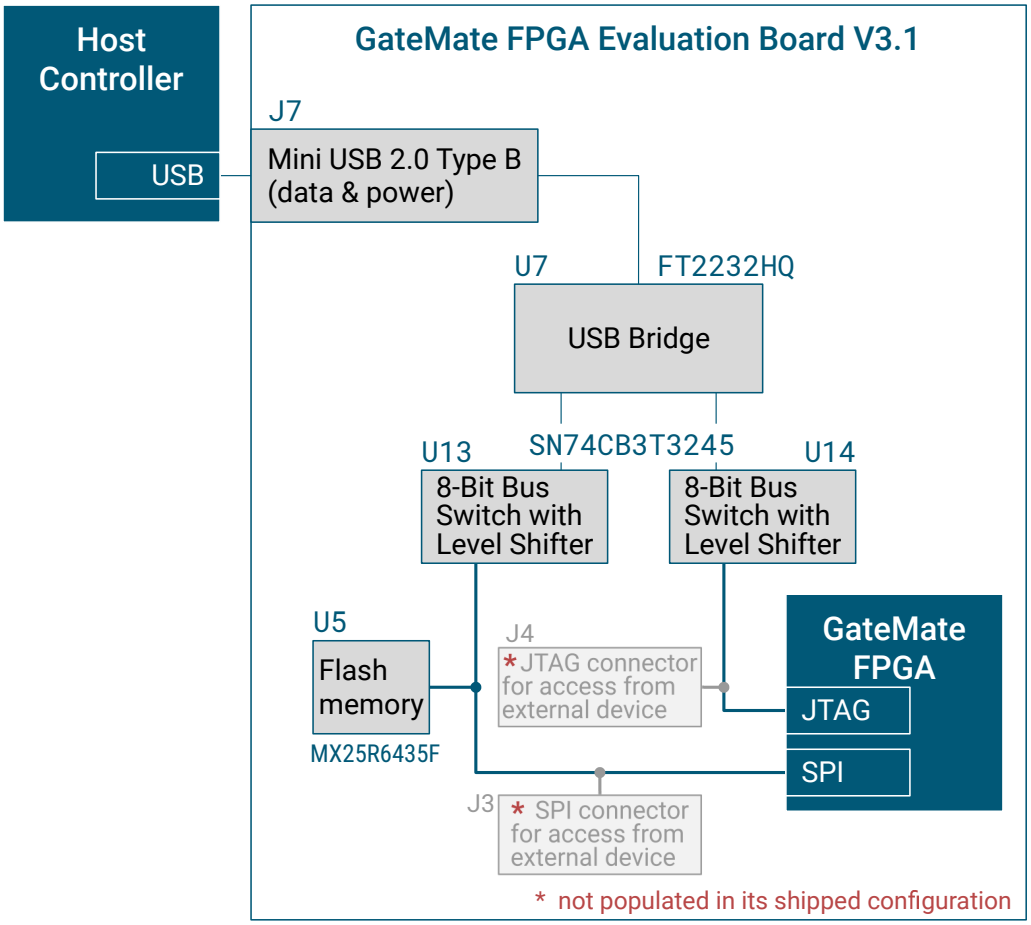


Figure 3.7: *Block diagram with details of SPI and JTAG interfaces*

The SPI bus can be accessed from any user device. For this, connector J3 (2.54 mm pin pitch, 9 pins) has to be populated. Figure 3.8 shows the pin assignment of the SPI connector.

The JTAG interface can be accessed from any user device. For this, connector J4 (2.54 mm pin pitch, 6 pins) has to be populated. Figure 3.9 shows the pin assignment of the JTAG connector.

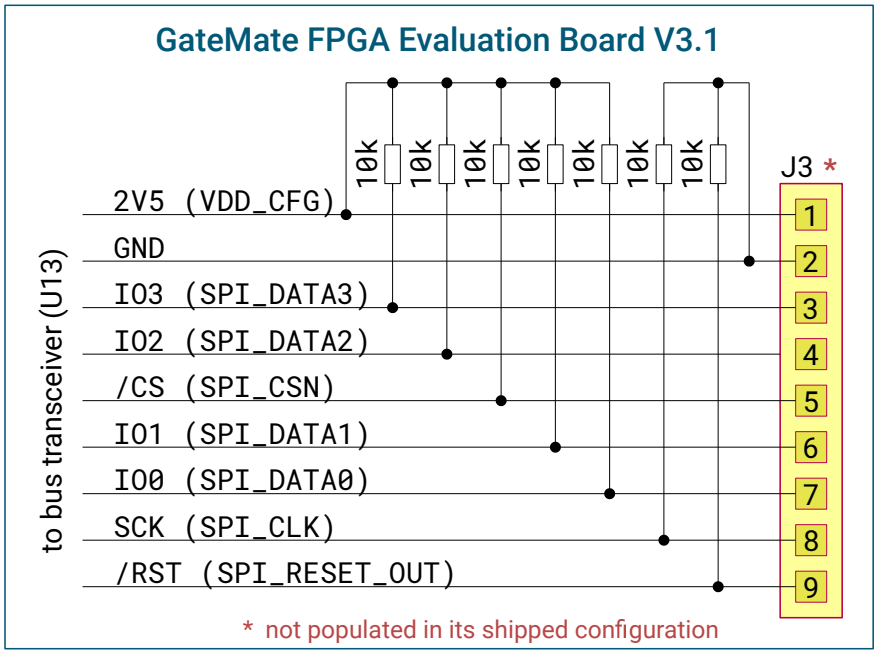


Figure 3.8: *Optional SPI interface connector J3*

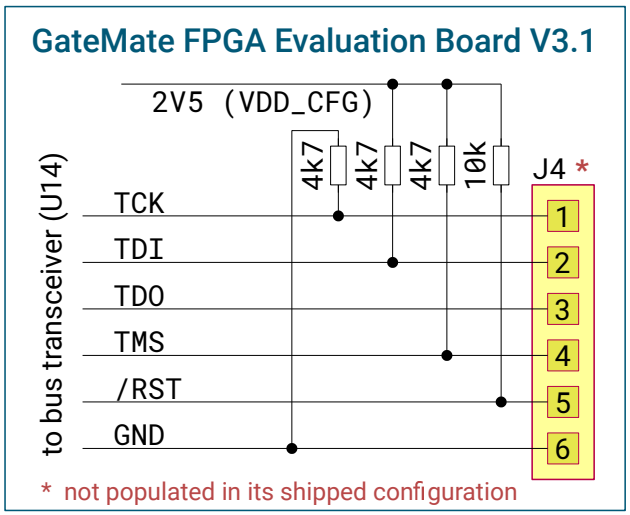


Figure 3.9: *Optional JTAG interface connector J4*

3.4 Configuration Mode and Reset

There are several ways to load the FPGA configuration. The configuration mode is choosen with switch SW1 setup as shown in Table 3.5.

Table 3.5: *GateMate^{TM} FPGA configuration modes*

CFG_MD[3:0] *		Configuration mode	
0x0	0b0000	SPI Master Mode	CPOL = 0, CPHA = 0
0x1	0b0001	SPI Master Mode	CPOL = 0, CPHA = 1
0x2	0b0010	SPI Master Mode	CPOL = 1, CPHA = 0
0x3	0b0011	SPI Master Mode	CPOL = 1, CPHA = 1
0x4	0b0100	SPI Slave Mode	CPOL = 0, CPHA = 0
0x5	0b0101	SPI Slave Mode	CPOL = 0, CPHA = 1
0x6	0b0110	SPI Slave Mode	CPOL = 1, CPHA = 0
0x7	0b0111	SPI Slave Mode	CPOL = 1, CPHA = 1
0xC	0b1100	JTAG	

* Modes not mentioned in the list may not be selected and lead to a malfunction of the device.

FPGA reset depends on different conditions:

- The user can press button SW2 to trigger FPGA reset.
- After power-on, all DC-DC converters must notify 'power good' to finish reset state.
- The host controller can trigger reset via SPI or JTAG interface. In this case either level shifter U13 or U14 will feed the host's reset signal to the GateMate^{TM} FPGA.
- An external SPI device can feed a reset signal to the FPGA via the SPI connector J3 pin 9 (see Figure 3.8).
- An external JTAG device can feed a reset signal to the FPGA via the JTAG connector J4 pin 5 (see Figure 3.9).
- The user application can trigger FPGA reset via GPIO bank connector J-C pin 41 (APP_RESET_OUT). This signal can be disabled via Jumper JP10.

The GPIO bank connector feeds a reset signal APP_RESET_IN to the user application. This is either the reset button SW2 or any reset condition mentioned above (see Figure 3.10).

Every GPIO bank connector has a APP_RESET_OUT signal. These are all connected together and are called 'User application reset out' in Figure 3.10.

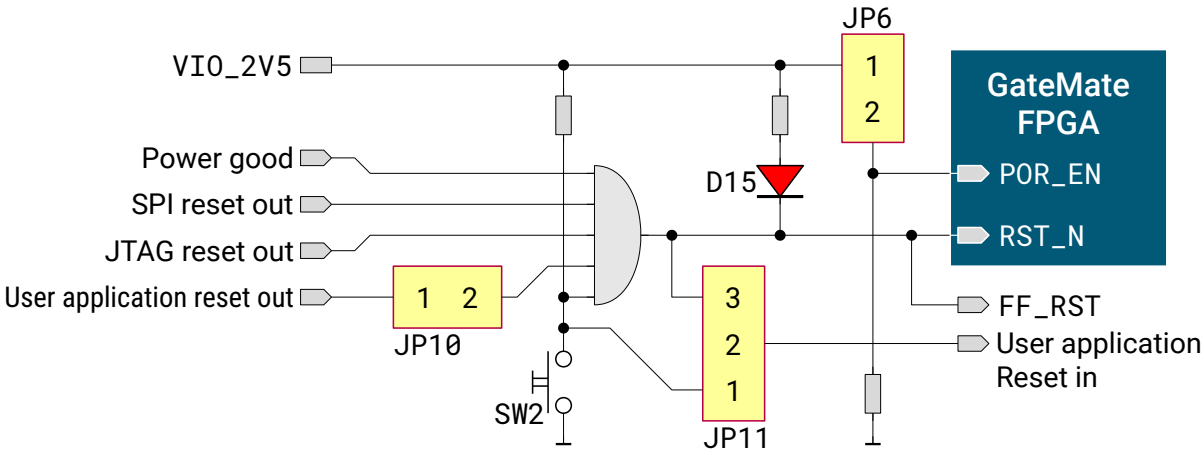


Figure 3.10: *Reset module*

After configuration, the GateMate™ FPGA reports whether the data stream was successfully loaded or not.

- LED D10 (green) is switched on when the data stream has completely been transferred.
- LED D9 (red) is switched on when an error occured.

Both signals are also passed to the host controller as shown in Figure 3.11. In case of an failed loading, a reset should be triggered in order to load the data stream again.

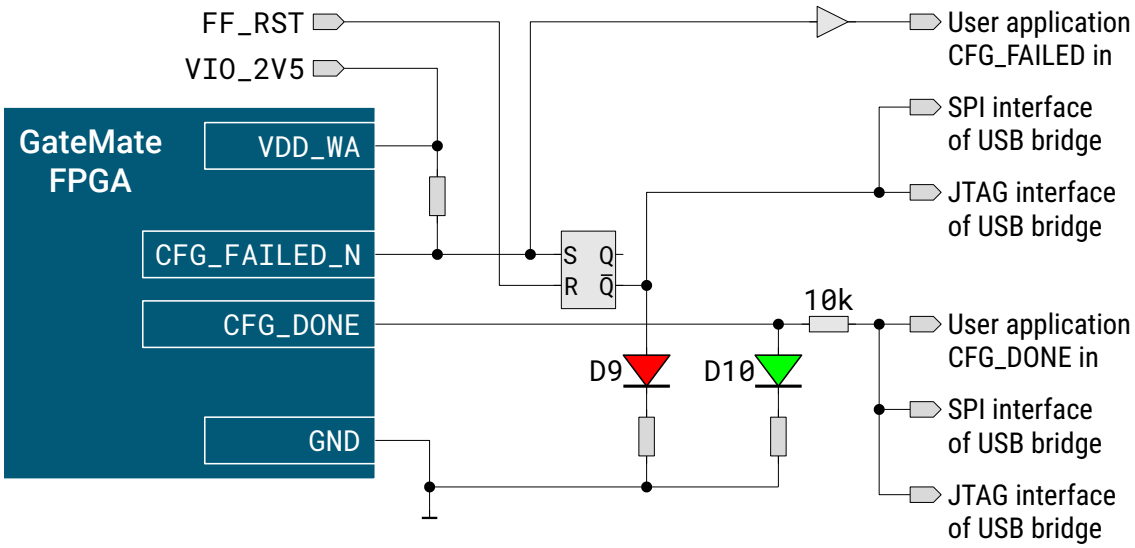


Figure 3.11: *Configuration status signals*

3.5 Clock Generation and Distribution

The evaluation board has an on-board oscillator X1 with 10.000 MHz frequency. This signal is connected to GPIO IO_SB_A8 which is the input for clock 0 (see Figure 3.12). The oscillator can be disabled with jumper JP8.

The GateMate™ FPGA has three more clock inputs connected to the GPIO WA bank. The evaluation board has these clocks prepared for usage, but some components have to be populated by the user as shown in Figure 3.14.

Clock 1: Another oscillator can be populated or an external clock source can be used via SMA jack J8.

Clock 2 and 3: The user application can feed two clock signals to the FPGA inputs. Jumpers JP1 and JP2 must be populated to select the clock source.

Finally, a low-voltage differential signaling (LVDS) clock oscillator can be populated to generate a Serializer / Deserializer (SerDes) input clock as shown in Figure 3.13. Please note, that also series resistors R73 and R74 have to be populated (see Figure 3.18 on page 38).

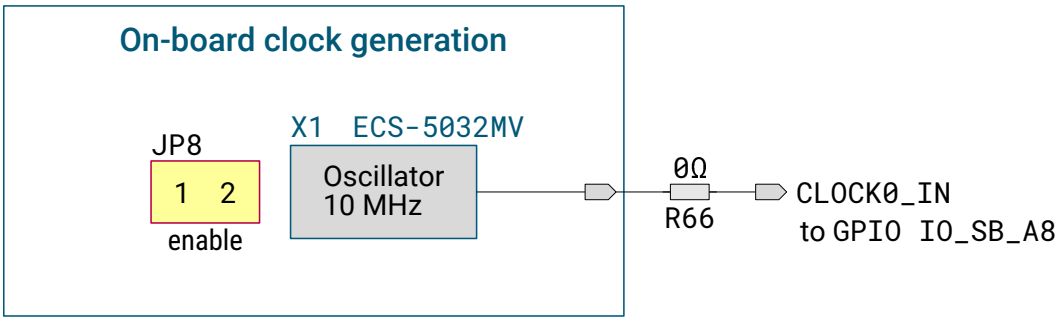


Figure 3.12: 10 MHz *on-board clock oscillator*

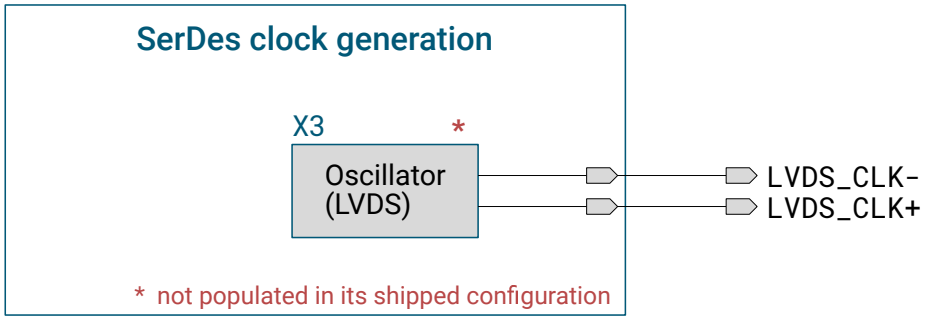


Figure 3.13: *Optional SerDes clock (LVDS clock oscillator)*

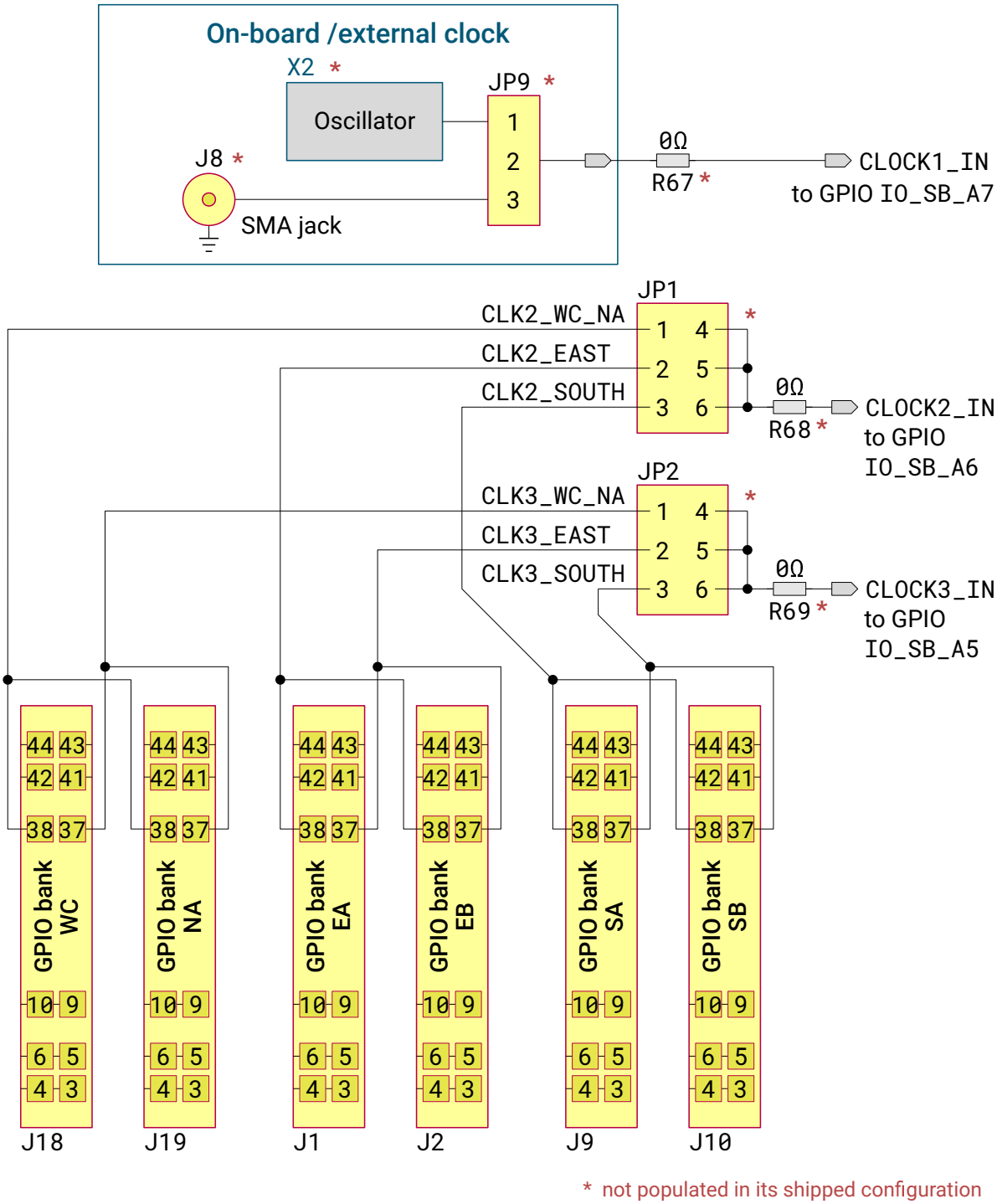


Figure 3.14: *Optional clock signals*

3.6 GPIO Connection to the User Application

The user application can be connected to one or more GPIO banks. Up to 6 banks are available. The other GPIO banks are assigned elsewhere.

All GPIO bank connectors have the same pinout as shown in Figure 3.15. Please note, that the GPIOs are arranged in two different ways with overturned signal vector. This is done to allow free choice of a GPIO bank for 1-bank user applications as shown in Figure 2.3 on page 17 and differential signal routing on the evaluation board at the same time. The PCB routing of all GPIO signals of banks EA and EB are inter-pair as well as intra-pair length matched. Details to the routing length are given in Table 3.8.

The user application can get it's power supply from the 3.3 V on-board DC-DC converter. In addition, GPIO voltage can be feed from the evaluation board to the user application or vice versa. Table 3.7 explains these VIOin and VIOout supply lines. The overall list of the GPIO bank connectors J-C is given in Table 3.6.

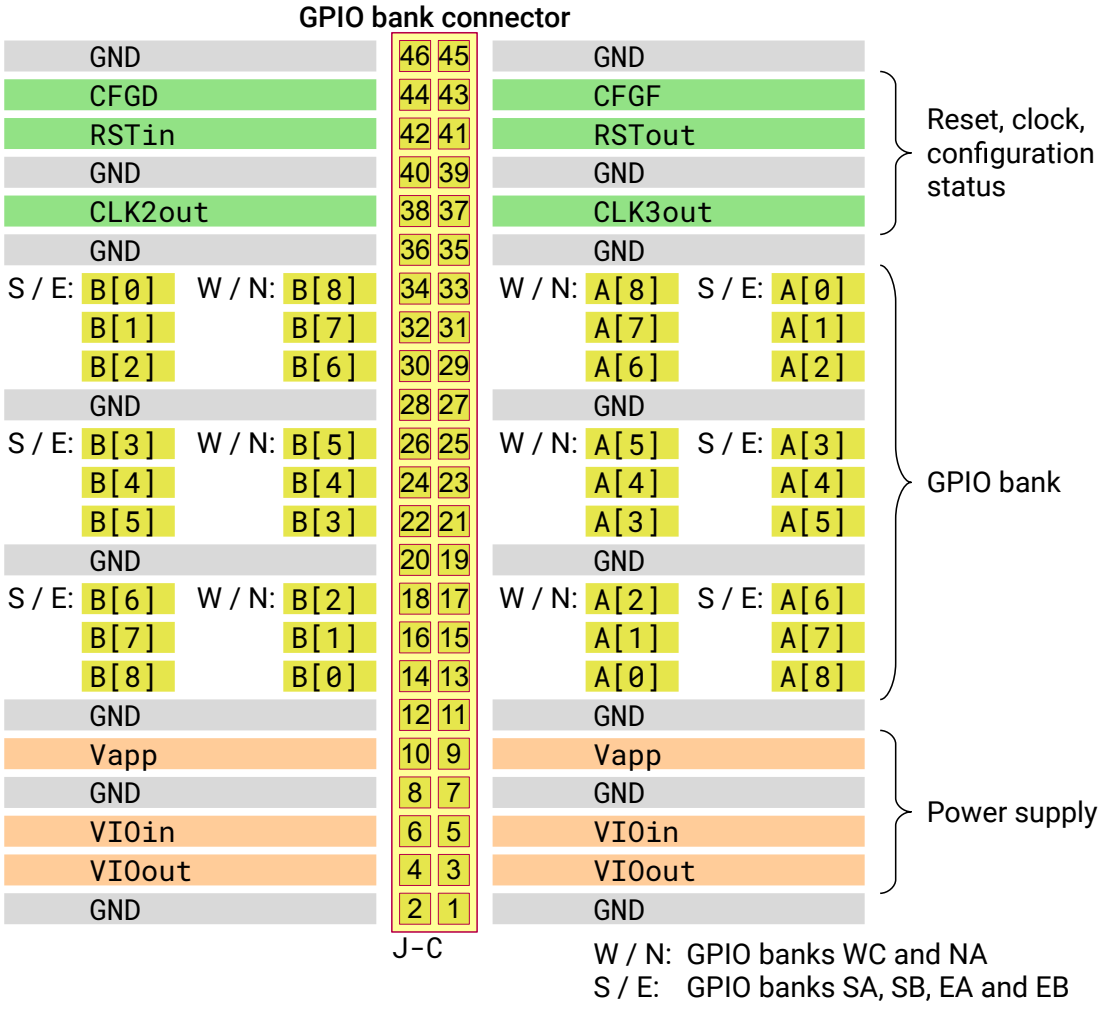


Figure 3.15: *GPIO bank connector J-C*

Table 3.6: *Pin assignment of GPIO connector J-C*

J-C pin	J-C signal	Schematic signal	Funktion
3 , 4	VIOout		see Table 3.7
5 , 6	VIOin		see Table 3.7
9 , 10	Vapp	VDD_APP	VIO_3V3 from power module
13 .. 33 [1]	A[8:0] or vice versa		to / from FPGA GPIO bank
14 .. 34 [2]	B[8:0] or vice versa		dto.
37	CLK3out		• 3 different signal pairs WC & NA, SA & SB and EA & EB from J-C connectors • to clock distribution jumper block JP2
38	CLK2out		• dto. • to clock distribution jumper block JP1
41	RSTout	APP_RESET_OUT	• from 6 GPIO connectors J-C • to reset circuitry via JP10
42	RSTin	APP_RESET_IN	• from JP11 of reset circuitry • to 6 GPIO connectors J-C
43	CFGF	CFG_FAILED_APP	• from FPGA pin CFG_FAILED_N • to 6 GPIO connectors J-C and FTDI chip (latched with flip-flop) via bus transceiver
44	CFGD	CFG_DONE_APP	• from FPGA pin CFG_DONE • to 6 GPIO connectors J-C and FTDI chip via bus transceiver

[1] odd only, pins 19 and 27 are GND
[2] even only, pins 20 and 28 are GND

Table 3.7: *Power input and output of GPIO connector J-C in Figures 3.4, 3.5 and 3.6 (pages 24 to 26)*

J-C	GPIO bank	VIOin	VIOout
J1	EA	from JP3 (selection)	to JP5, supply option for FPGA GPIO banks
J2	EB	dto.	dto.
J9	SA	VIO_2V5 from power module	not connected
J10	SB	dto.	dto.
J18	WC	from JP15 (selection)	to JP16, supply option for FPGA GPIO banks
J19	NA	dto.	dto.

Table 3.8: *Maximum intra-pair and inter-pair length mismatch of the GPIO banks*

GPIO bank	Intra-pair length mismatch	Inter-pair length mismatch
EA *	0.9 mm	2.0 mm
EB *	1.8 mm	1.8 mm
SA	3.4 mm	11.7 mm
SB	3.6 mm	13.0 mm
NA	4.9 mm	12.1 mm
WC	5.3 mm	14.4 mm

* Best fit. Recommended for high speed applications.

3.7 Pmod Interface

GPIO bank NB constitudes a Pmod interface with two standard 12-pin connectors J17A and J17B.

Supply voltage 3.3 V should be selected via jumper JP14 to fulfill Pmod specification. If desired for certain applications, 2.5 V supply can be choosen exceptionally. Please note, that many Pmod devices will not work properly in this case.

Table 3.9 shows the GPIO signals connected to the Pmod interface connectors J17A and J17B.

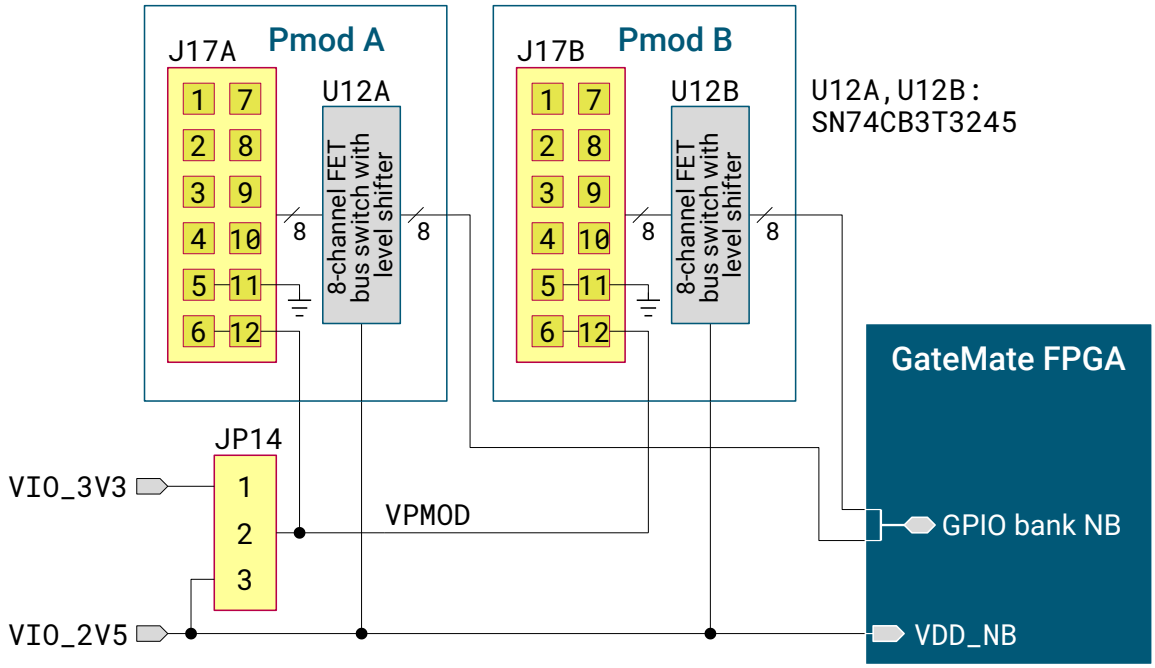


Figure 3.16: *GPIO bank NB with Pmod interface*

Table 3.9: *Pmod signal assignment of J17A and J17B connectors*

J17A/B pin	Pmod signal	GPIO for Pmod A	GPIO for Pmod B	J17A/B pin	Pmod signal	GPIO for Pmod A	GPIO for Pmod B
1	IO1	IO_NB_A0	IO_NB_A4	7	IO2	IO_NB_B0	IO_NB_B4
2	IO3	IO_NB_A1	IO_NB_A5	8	IO4	IO_NB_B1	IO_NB_B5
3	IO5	IO_NB_A2	IO_NB_A6	9	IO6	IO_NB_B2	IO_NB_B6
4	IO7	IO_NB_A3	IO_NB_A7	10	IO8	IO_NB_B3	IO_NB_B7
5	GND			11	GND		
6	VPMOD			12	VPMOD		

3.8 HyperRAM Device

GPIO bank WB is used to provide an on-board HyperRAM memory (see Figure 3.17). U10 is a 64 Mb device which is connected to the GPIO bank as shown in Table 3.10.

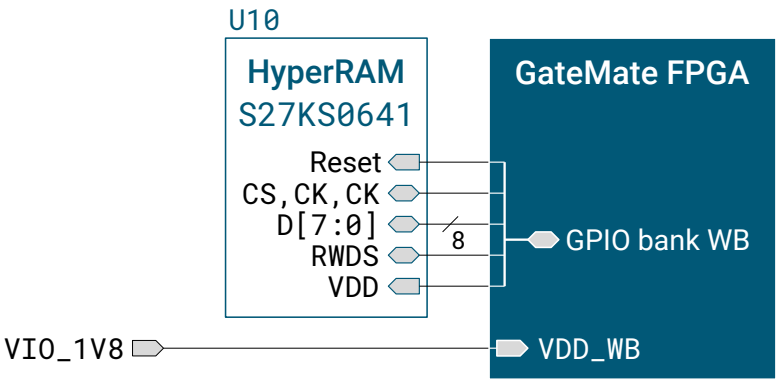


Figure 3.17: *GPIO bank WB with HyperRAM device*

Table 3.10: *GPIO assignment to the on-board HyperRAM device*

GPIO	HyperRAM signal	GPIO	HyperRAM signal
IO_WB_A0	–	IO_WB_B0	$\overline{CS}$
IO_WB_A1	–	IO_WB_B1	–
IO_WB_A2	$\overline{RESET}$	IO_WB_B2	–
IO_WB_A3	CK	IO_WB_B3	$\overline{CK}$
IO_WB_A4	–	IO_WB_B4	RWDS
IO_WB_A5	DQ0	IO_WB_B5	DQ1
IO_WB_A6	DQ2	IO_WB_B6	DQ3
IO_WB_A7	DQ4	IO_WB_B7	DQ5
IO_WB_A8	DQ6	IO_WB_B8	DQ7

3.9 SerDes Interface

The evaluation board is prepared to offer a SerDes interface. Figure 3.18 shows, that the SMA jacks J13 . . J16 must be populated from the user to get access to the CCGM1A1 SerDes interface.

There are two ways to feed in the SerDes clock signal:

1. SMA jacks J11 and J12 are populated to feed in an external LVDS clock.
2. An on-board LVDS oscillator and the series resistors R73 and R74 are populated (see also Figure 3.13 on page 31).

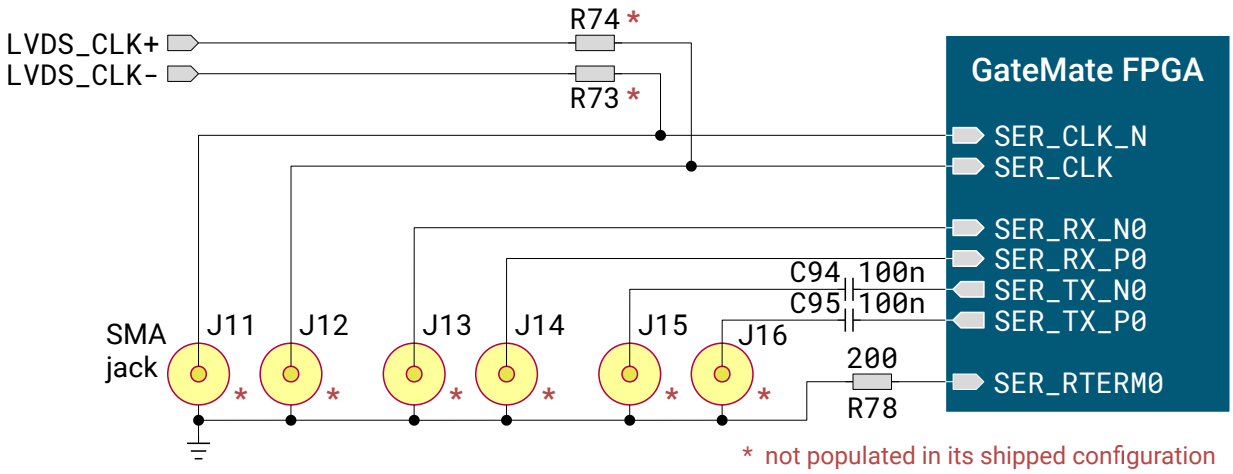


Figure 3.18: *Optional SerDes interface*

Chapter 4

Electrical Characteristics

Table 4.1: *Absolute maximum characteristics of the GateMate^{TM} FPGA evaluation board*

Symbol	Min	Typ	Max	Unit	Description
	-40		125	°C	Junction temperature
V_{in}	-0.3		6.5	V	Power supply from J5 or J6
V_{in}	-0.3		6.0	V	Power supply from J7
T_{stg}	-55		150	°C	Storage temperature

Table 4.2: *Operating characteristics of the GateMate^{TM} FPGA evaluation board*

Symbol	Min	Typ	Max	Unit	Description
	-40		85	°C	Operating temperature
V_{in}	4.0		6.0	V	Power supply from J5 or J6
V_{in}	4.75		5.75	V	Power supply from J7
I_{in}		140		mA	Power consumption during reset

Table 4.3: *GPIO characteristics in single-ended mode*

Symbol	Min	Typ	Max	Unit	Description
VDD_{IO}	1.1		2.7	V	I/O supply voltage (GPIO banks and VDD_CLK)
V_{IN}	-0.4		VDD_{IO} +0 4	V	Input voltage range
Schmitt-trigger function disabled:					
V_{IH}	0.43		0.51	VDD_{IO}	Input high threshold voltage
V_{IL}	0.45		0.51	VDD_{IO}	Input low threshold voltage
V_{HYST}		0		V	Hysteresis
Schmitt-trigger function enabled:					
V_{IH}	0.61		0.67	VDD_{IO}	Input high threshold voltage
V_{IL}	0.31		0.39	VDD_{IO}	Input low threshold voltage
V_{HYST}	0.26		0.33	VDD_{IO}	Hysteresis
Output driver disabled:					
I_{IL}			1	µA	Input pin current when driven active low
I_{IH}			1	µA	Input pin current when driven active high
R_{PU}		50		kΩ	Pull-up resistance
R_{PD}		50		kΩ	Pull-down resistance
$I_{DD, max}$			158	µA	Maximum supply current at GPIO input at transition point

Table 4.4: *GPIO characteristics in LVDS mode*

Symbol	Min	Typ	Max	Unit	Description
VDD_{IO}	1.62		2.75	V	I/O supply voltage
I_{out}		3.2		mA	Output current when LVDS output current boost is set to nominal current
I_{out}		6.4		mA	Output current when LVDS output current boost is set to increased output current
VCM_{TX}		$VDD_{IO}/2$		V	Common-mode voltage
R_{term}	90	100	130	Ω	

Chapter 5

Mechanical Dimensions

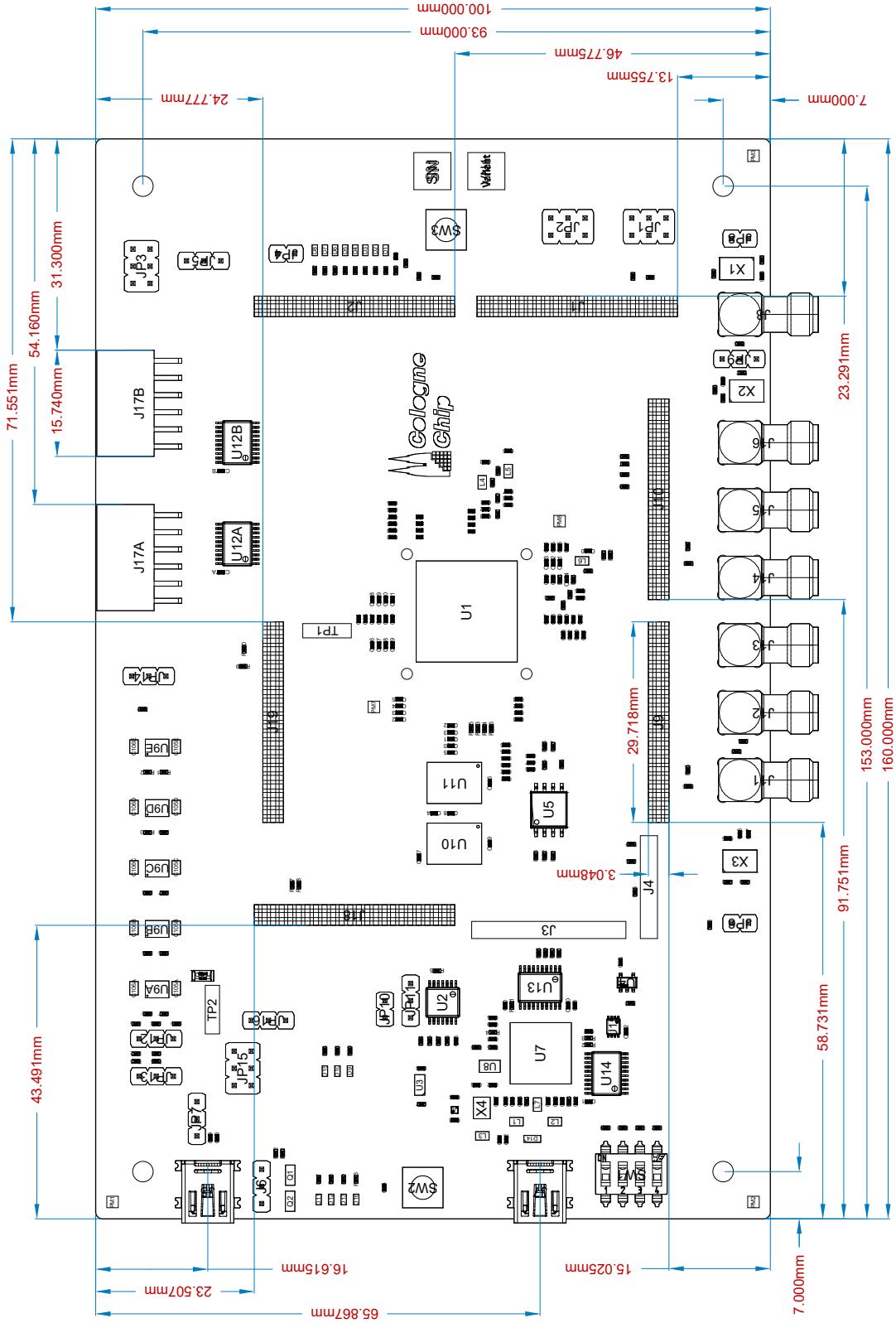


Figure 5.1: *Board dimensions and position of connectors*

Appendix A

Summary Overviews

A.1 PCB components

Figure A.1 points out partial circuits that have been described in the previous chapters. The corresponding Table A.1 lists all associated Figures and where they can be found in this document.

Table A.1: *Component locations on the GateMate™ FPGA evaluation board (numbering in counter clockwise order)*

Marking	Function	Shown in Fig.	on Page
1	FPGA core voltage	3.3	22
2	PCB power supply	3.1	21
3	GPIO supply voltage selection (banks WC and NA)	3.4	24
4	Configuration status (LEDs for CFG_DONE and CFG_FAILED_N)	3.11	30
5	Reset	3.10	30
6	HyperRam device	3.17	37
7	USB bridge	3.7	27
8	Flash memory	3.7	27
9	SPI interface	3.7, 3.8	27, 28
10	JTAG interface	3.7, 3.9	27, 28
11	Configuration mode setup	Tab. 3.5	29
12	Power-on reset (POR) enable	3.10	30
13	SerDes LVDS clock	3.13	31
14	SerDes interface	3.18	38
15	GateMate™ FPGA CCGM1A1	1.1	12
16	On-board oscillator CLOCK0_IN	3.12	31
17	Optional clock signals CLOCK1_IN ..CLOCK3_IN	3.14	32
18	GPIO supply voltage selection (banks EA and EB) with alternative LEDs and push button on bank EB	3.4	24
19	Pmod interface	3.16	36

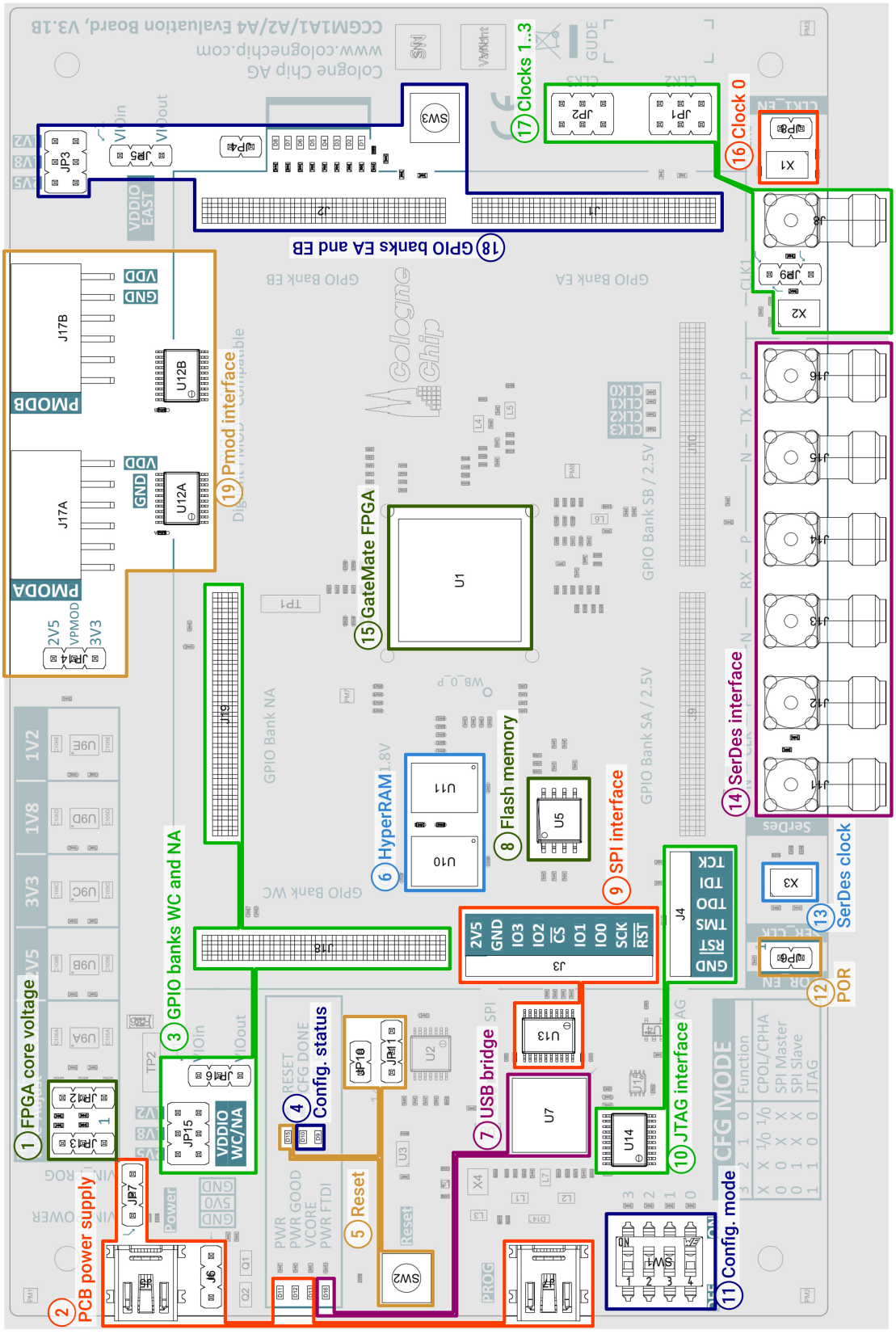


Figure A.1: *Component locations on the GateMate™ FPGA evaluation board*

A.2 Default Jumper Settings

Table A.2: *Default jumper settings*

Designator	Color	Function	Default	Shown in Fig.	on Page
JP1 *	black	Clock distribution from user application to FPGA CLOCK2 signal.	–	3.14	32
JP2 *	black	Clock distribution from user application to FPGA CLOCK3 signal.	–	3.14	32
JP3	blue	Select supply voltage for GPIO banks EA and EB and user application supply input VIOin (1.2 V, 1.8 V or 2.5 V).	5-6: 2.5 V	3.5	25
JP4	black	Enable LEDs on GPIO bank EB.	closed	3.5	25
JP5	blue	Select supply voltage for GPIO banks EA and EB (from JP3 or user application supply output VIOout).	1-2: JP3	3.5	25
JP6	black	Enable power-on reset (POR) module.	closed	3.10	30
JP7	red	Power source selection from J5 or J7.	2-3: J7	3.1	21
JP8	black	Oscillator enable for CLOCK0 signal.	closed	3.12	31
JP9 *	black	CLOCK1 source selection from on-board oscillator * or external source via SMA jack J8. *	–	3.14	32
JP10	black	Enable reset signal from user application.	opened	3.10	30
JP11	black	Select reset signal input of user application (reset button only or any board reset).	opened	3.10	30
JP12	red	Core voltage level adjustment (low power, economy or speed mode).	1-2: econ.	3.3	22
JP13	red	Core voltage fine tuning (min, typ, max).	1-2: typ	3.3	22
JP14	red	Select Pmod supply voltage 3.3 V or 2.5 V.	1-2: 3.3 V	3.16	36
JP15	blue	Select supply voltage for GPIO banks NA and WC and user application supply input VIOin (1.2 V, 1.8 V or 2.5 V).	5-6: 2.5 V	3.4	24
JP16	blue	Select supply voltage for GPIO banks NA and WC (from JP15 or user application supply output VIOout).	1-2: JP15	3.4	24

* Not populated in its shipped configuration.

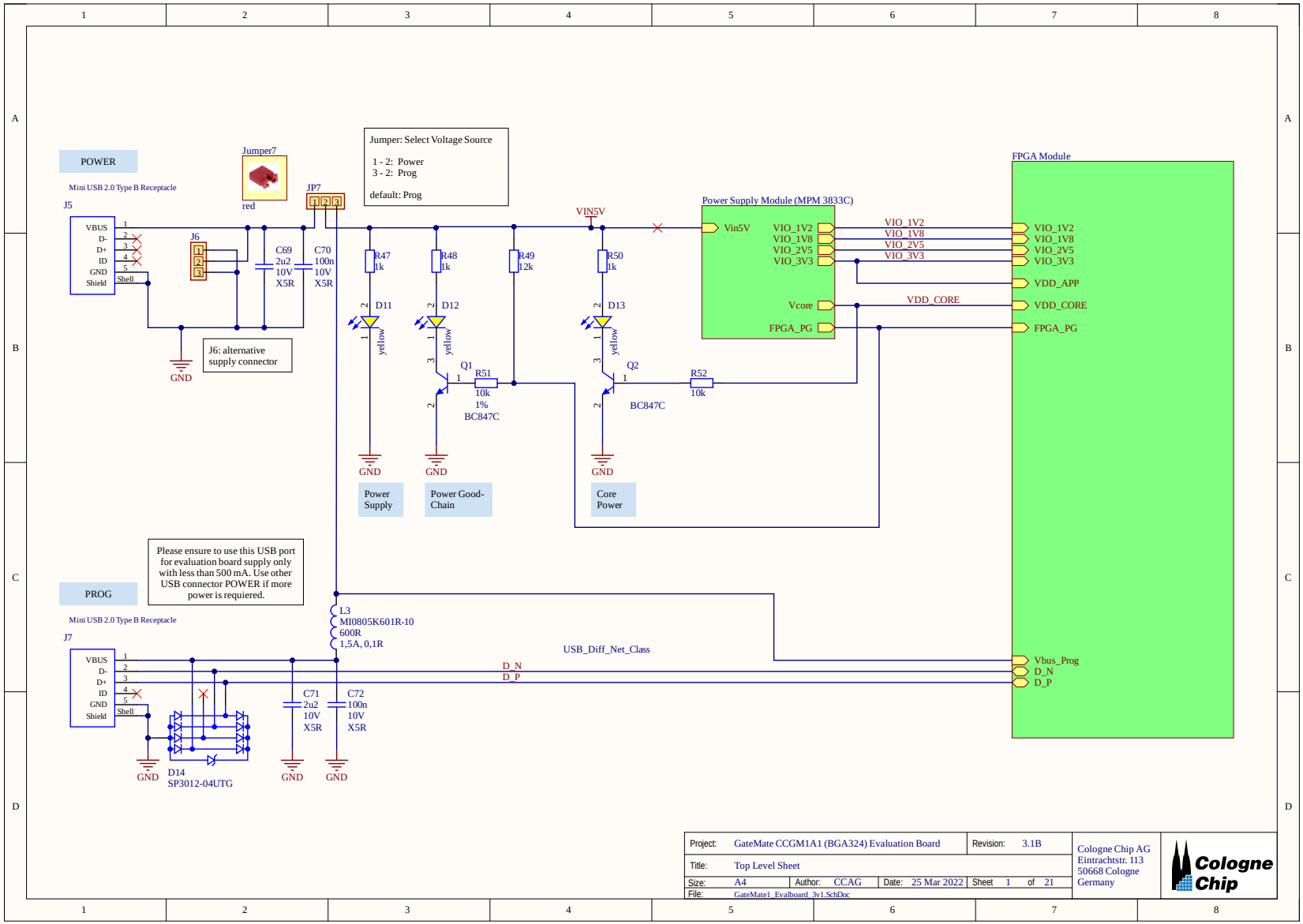
A.3 LEDs and Push Buttons

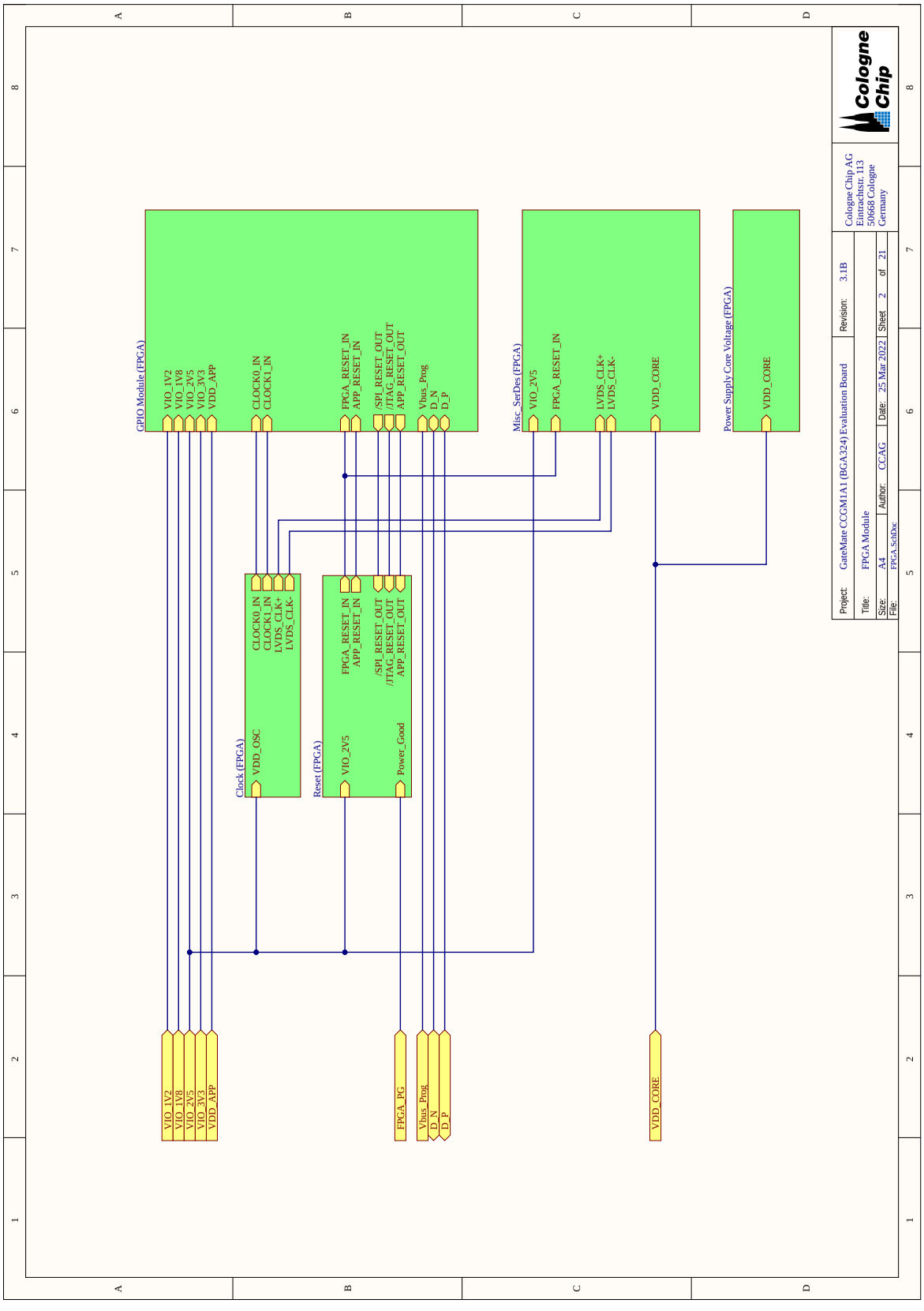
Table A.3: *LEDs and push buttons*

Designator	Color	Function	Shown in Fig.	on Page
D1 . . D8	green	User LEDs assigned to GPIO bank EB	3.5	25
D9	red	Configuration state CFG_FAILED_N	3.11	30
D10	green	Configuration state CFG_DONE	3.11	30
D11	yellow	PCB power supply	3.1	21
D12	yellow	Power good notification from on-board DC-DC converters	3.1	21
D13	yellow	FPGA core power	3.1	21
D15	red	FPGA reset	3.10	30
D16	yellow	Power supply from USB data jack J7 (supply for U7, FT2232HQ-Tray)	2.1, 3.7	15, 27
SW2	red	PCB reset	3.10	30
SW3	black	User button assigned to GPIO bank EB	3.5	25

Appendix B

Evaluation Board Schematics


POWER
Mini USB 2.0 Type B Receptacle
J5
VBUS
D-
D+
ID
GND
Shield
Shell
Jumper7
red
JP7
J6
C69
2u2
10V
X5R
C70
100n
10V
X5R
GND
J6: alternative supply connector
Jumper: Select Voltage Source
1 - 2: Power
3 - 2: Prog
default: Prog
VIN5V
R47
1k
R48
1k
R49
12k
R50
1k
D11
D12
D13
yellow
Q1
Q2
R51
10k
1%
BC847C
R52
10k
BC847C
Power Supply
Power Good-Chain
Core Power
Power Supply Module (MPM 3833C)
Vin5V
VIO_1V2
VIO_1V8
VIO_2V5
VIO_3V3
Vcore
FPGA_PG
VDD_CORE
FPGA Module
VIO_1V2
VIO_1V8
VIO_2V5
VIO_3V3
VDD_APP
VDD_CORE
FPGA_PG
Please ensure to use this USB port for evaluation board supply only with less than 500 mA. Use other USB connector POWER if more power is requiered.
PROG
Mini USB 2.0 Type B Receptacle
J7
L3
MI0805K601R-10
600R
1,5A, 0,1R
USB_Diff_Net_Class
D_N
D_P
Vbus_Prog
C71
2u2
10V
X5R
C72
100n
10V
X5R
D14
SP3012-04UTG
Project: GateMate CCGM1A1 (BGA324) Evaluation Board
Revision: 3.1B
Title: Top Level Sheet
Size: A4
Author: CCAG
Date: 25 Mar 2022
Sheet 1 of 21
File: GateMate1_Evalboard_3v1.SchDoc
Cologne Chip AG
Eintrachtstr. 113
50668 Cologne
Germany


GPIO Module (FPGA)
VIO_1V2
VIO_1V8
VIO_2V5
VIO_3V3
VDD_APP
CLOCK0_IN
CLOCK1_IN
FPGA_RESET_IN
APP_RESET_IN
SPI_RESET_OUT
/JTAG_RESET_OUT
APP_RESET_OUT
Vbus_Prog
D_N
D_P
Misc_SerDes (FPGA)
VIO_2V5
FPGA_RESET_IN
LVDS_CLK+
LVDS_CLK-
VDD_CORE
Power Supply Core Voltage (FPGA)
VDD_CORE
Clock (FPGA)
VDD_OSC
CLOCK0_IN
CLOCK1_IN
LVDS_CLK+
LVDS_CLK-
Reset (FPGA)
VIO_2V5
FPGA_RESET_IN
APP_RESET_IN
/SPI_RESET_OUT
/JTAG_RESET_OUT
APP_RESET_OUT
Power_Good
FPGA_PG
Project: GateMate CCGM1A1 (BGA324) Evaluation Board
Revision: 3.1B
Title: FPGA Module
Size: A4
Author: CCAG
Date: 25 Mar 2022
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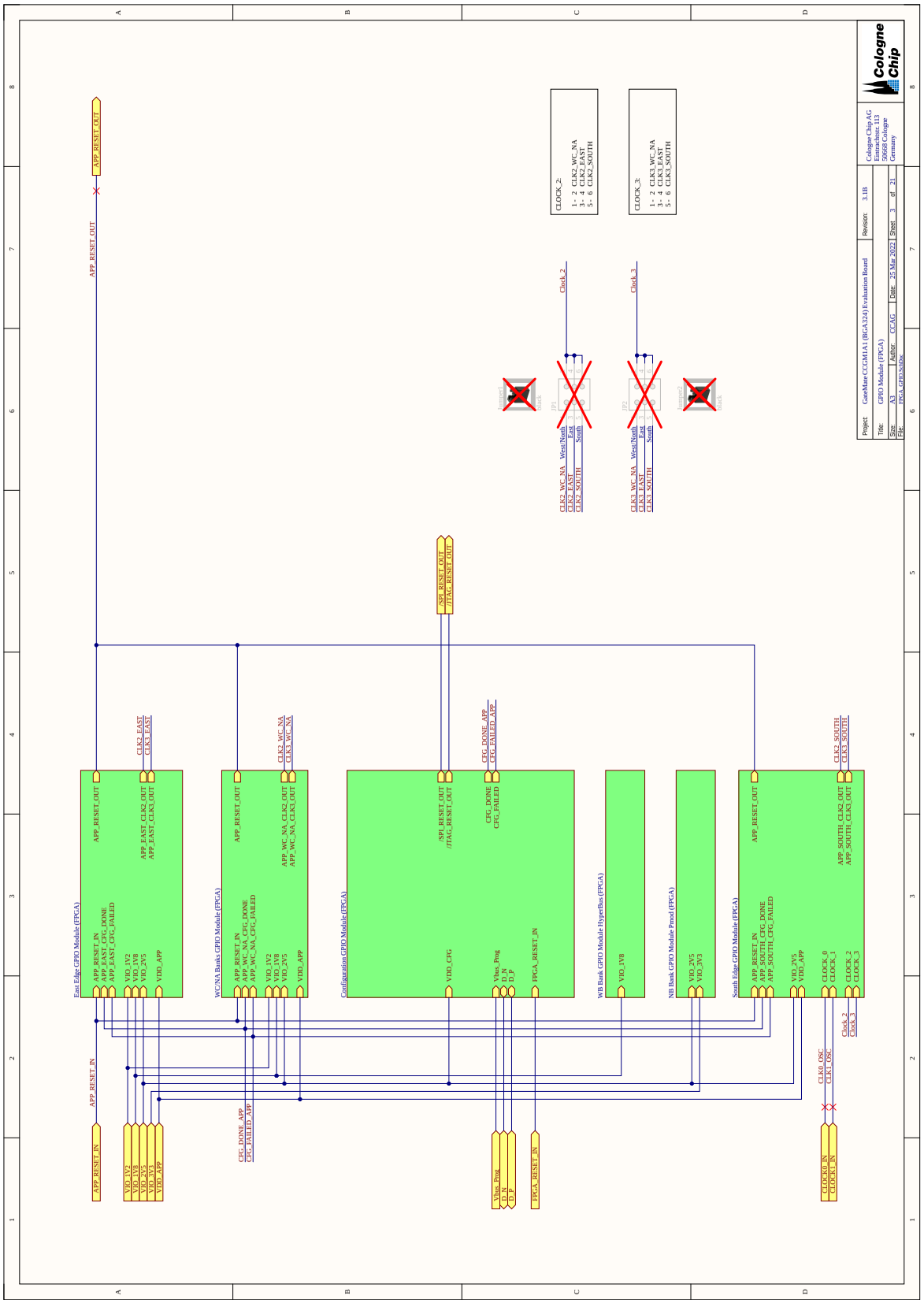
Eintrachtstr. 113
50668 Cologne
Germany


APP_RESET_OUT
CLOCK_2:
1 - 2 CLK2_WC_NA
3 - 4 CLK2_EAST
5 - 6 CLK2_SOUTH
CLOCK_3:
1 - 2 CLK3_WC_NA
3 - 4 CLK3_EAST
5 - 6 CLK3_SOUTH
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Revision: 3.1B
Title: GPIO Module (FPGA)
Size: A3
Author: CCAG
Date: 25 Mar 2022
Sheet 3 of 21
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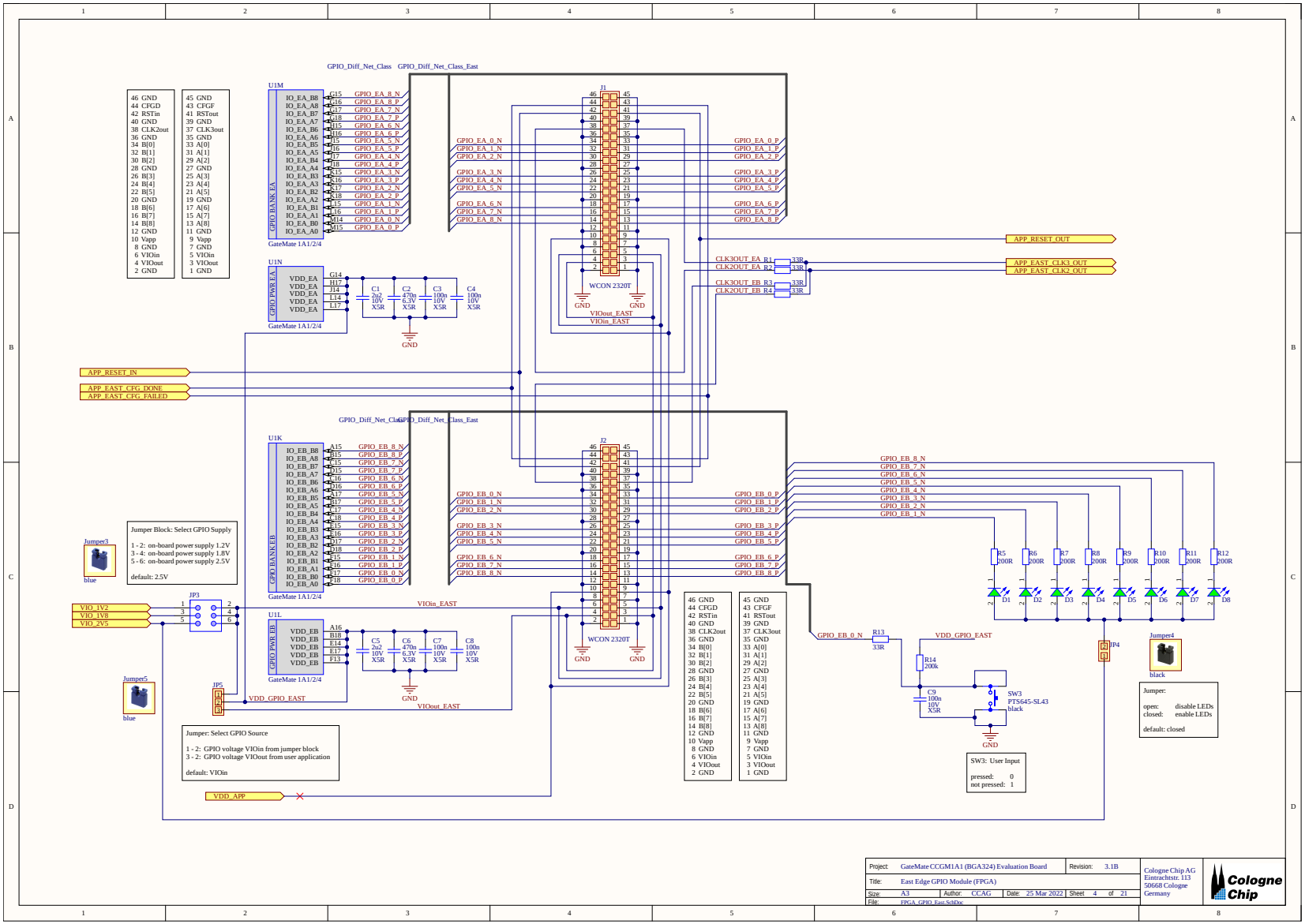
Cologne Chip AG
Einrichstrasse 113
50668 Cologne
Germany
East Edge GPIO Module (FPGA)
WC/NA Banks GPIO Module (FPGA)
Configuration GPIO Module (FPGA)
WB Bank GPIO Module HyperBus (FPGA)
NB Bank GPIO Module Pmod (FPGA)
South Edge GPIO Module (FPGA)
SPI_RESET_OUT
JTAG_RESET_OUT
CFG_DONE_APP
CFG_FAILED_APP
APP_RESET_IN
FPGA_RESET_IN
CLK0_OSC
CLK1_OSC
CLOCK0_IN
CLOCK1_IN


GPIO_Diff_Net_Class GPIO_Diff_Net_Class_East
U1M
GPIO BANK 6A
GateMate 1A1/2/4
U1N
GPIO PWR 6A
U1K
GPIO BANK 6B
U1L
GPIO PWR 6B
J1
J2
WCON 2320T
VIOout_EAST
VIOin_EAST
APP_RESET_IN
APP_EAST_CFG_DONE
APP_EAST_CFG_FAILED
APP_RESET_OUT
APP_EAST_CLK3_OUT
APP_EAST_CLK2_OUT
Jumper3
Jumper Block: Select GPIO Supply
1 - 2: on-board power supply 1.2V
3 - 4: on-board power supply 1.8V
5 - 6: on-board power supply 2.5V
default: 2.5V
JP3
VIO_1V2
VIO_1V8
VIO_2V5
Jumper5
JP5
Jumper: Select GPIO Source
1 - 2: GPIO voltage VIOin from jumper block
3 - 2: GPIO voltage VIOout from user application
default: VIOin
VDD_APP
VDD_GPIO_EAST
R13
R14 200k
C9 100n 10V X5R
SW3 PTS645-SL43 black
SW3: User Input
pressed: 0
not pressed: 1
JP4
Jumper4
Jumper:
open: disable LEDs
closed: enable LEDs
default: closed
Project: GateMate CCGM1A1 (BGA324) Evaluation Board
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Title: East Edge GPIO Module (FPGA)
Size: A3
Author: CCAG
Date: 25 Mar 2022
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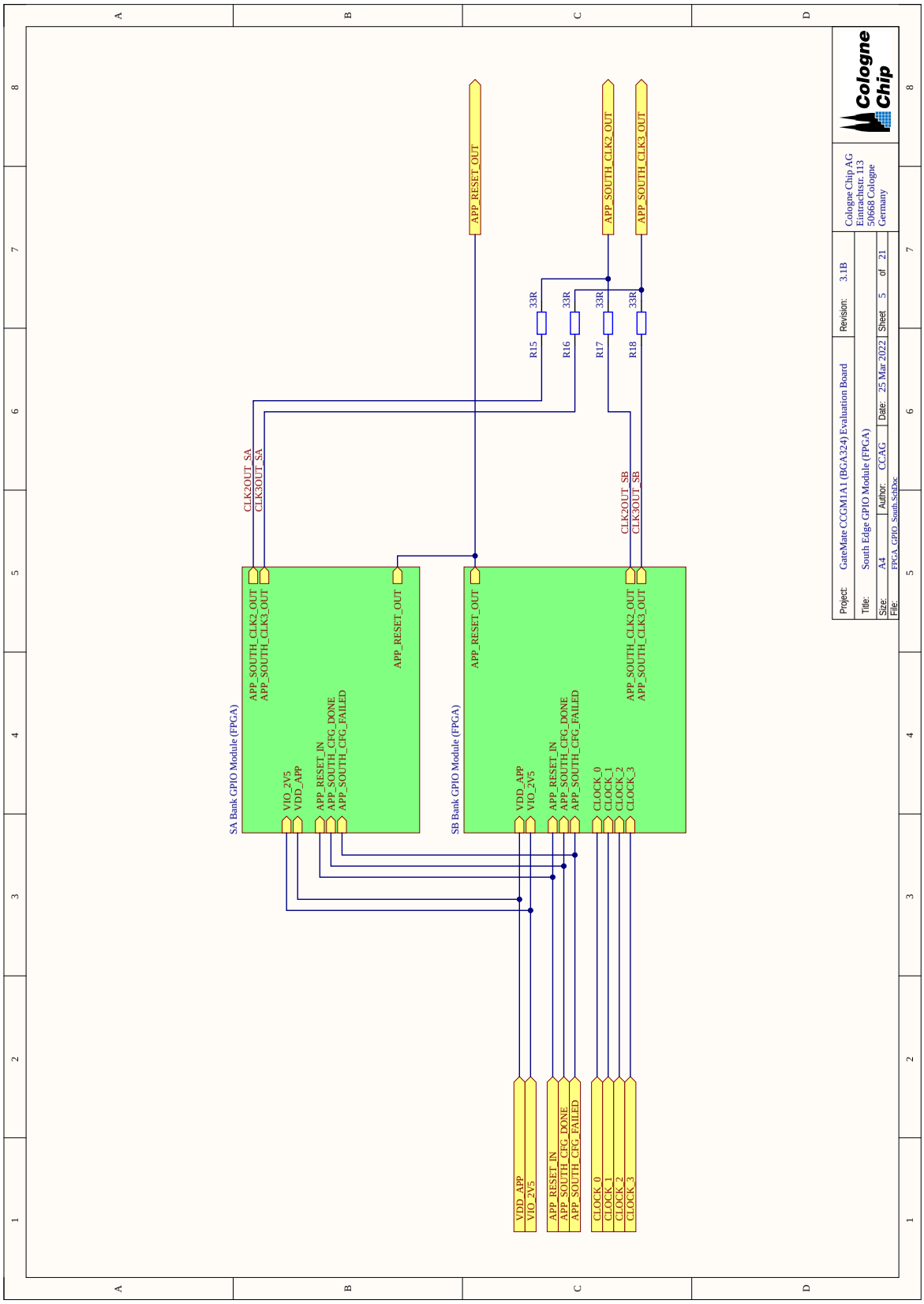
APP_RESET_OUT
APP_SOUTH_CLK2_OUT
APP_SOUTH_CLK3_OUT
R15 33R
R16 33R
R17 33R
R18 33R
CLK2OUT_SA
CLK3OUT_SA
CLK2OUT_SB
CLK3OUT_SB
SA Bank GPIO Module (FPGA)
APP_SOUTH_CLK2_OUT
APP_SOUTH_CLK3_OUT
APP_RESET_OUT
VIO_2V5
VDD_APP
APP_RESET_IN
APP_SOUTH_CFG_DONE
APP_SOUTH_CFG_FAILED
SB Bank GPIO Module (FPGA)
APP_RESET_OUT
APP_SOUTH_CLK2_OUT
APP_SOUTH_CLK3_OUT
VDD_APP
VIO_2V5
APP_RESET_IN
APP_SOUTH_CFG_DONE
APP_SOUTH_CFG_FAILED
CLOCK_0
CLOCK_1
CLOCK_2
CLOCK_3
VDD_APP
VIO_2V5
APP_RESET_IN
APP_SOUTH_CFG_DONE
APP_SOUTH_CFG_FAILED
CLOCK_0
CLOCK_1
CLOCK_2
CLOCK_3
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Size: A4
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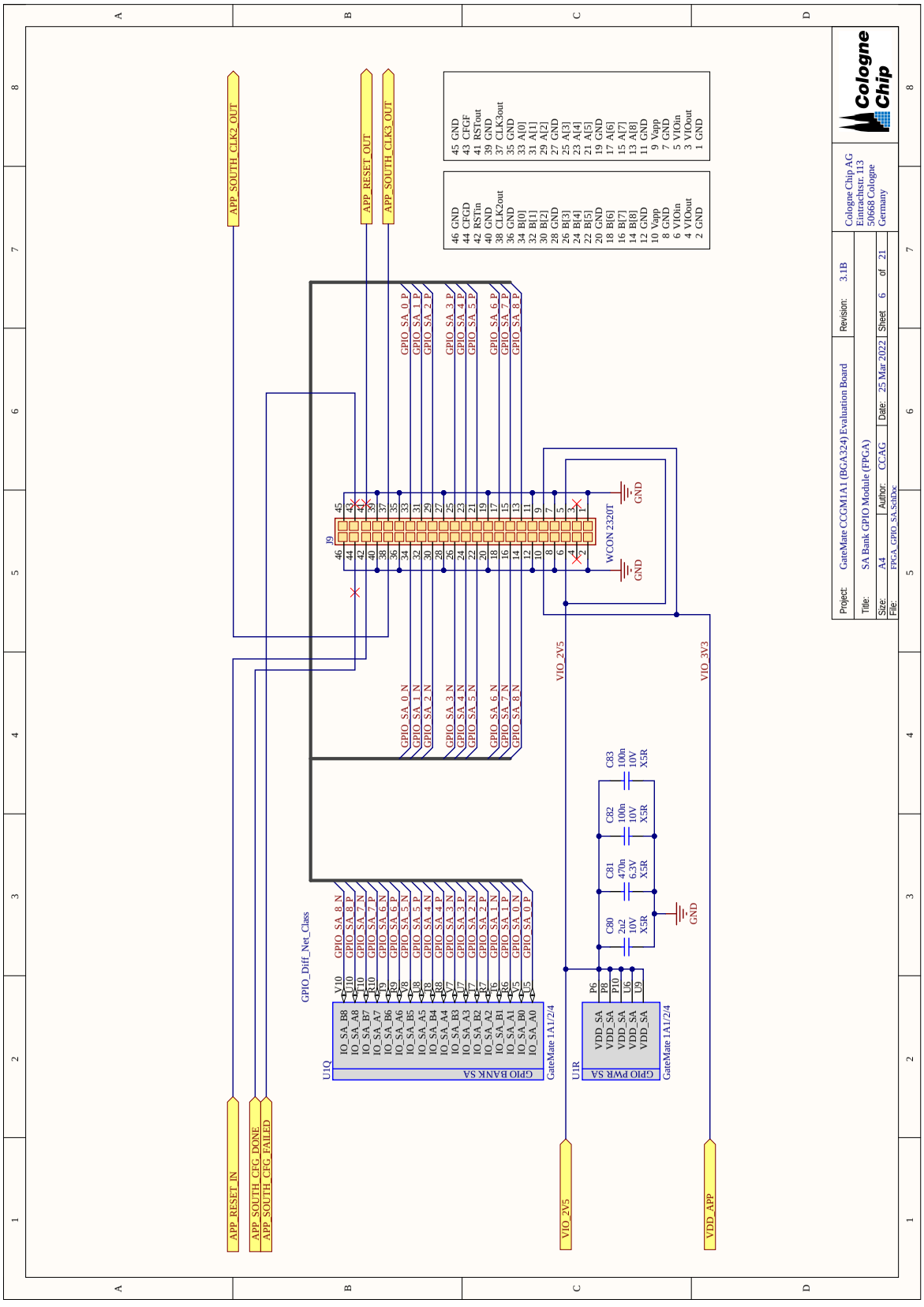
APP_SOUTH_CLK2_OUT
APP_RESET_OUT
APP_SOUTH_CLK3_OUT
APP_RESET_IN
APP_SOUTH_CFG_DONE
APP_SOUTH_CFG_FAILED
VIO_2V5
VIO_3V3
VDD_APP
J9
WCON 2320T
GND
GPIO_Diff_Net_Class
U1Q
GPIO BANK 5A
GateMate 1A1/2/4
U1R
GPIO PWR 5A
C80
C81
C82
C83
Project: GateMate CCGM1A1 (BGA324) Evaluation Board
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Size: A4
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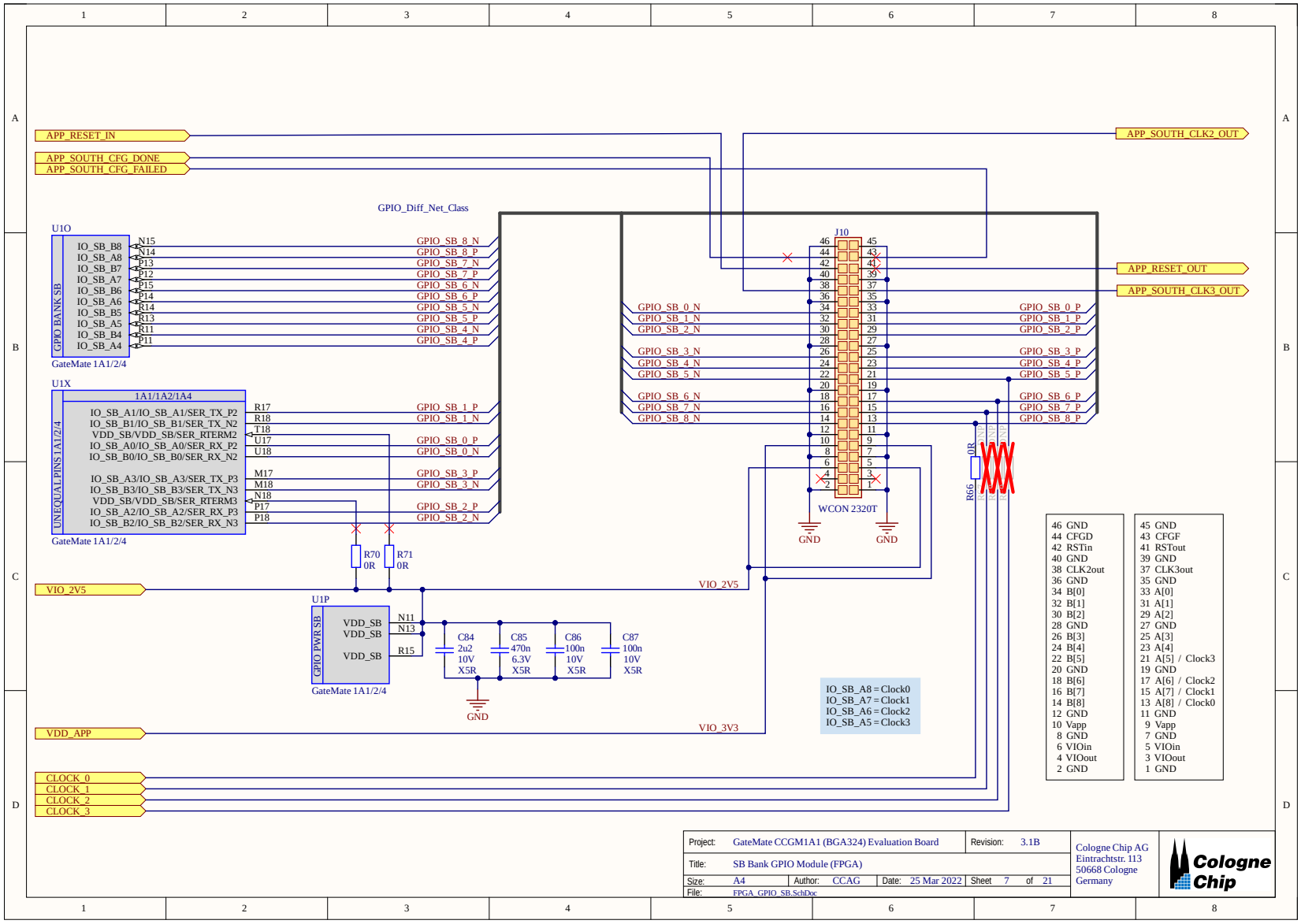
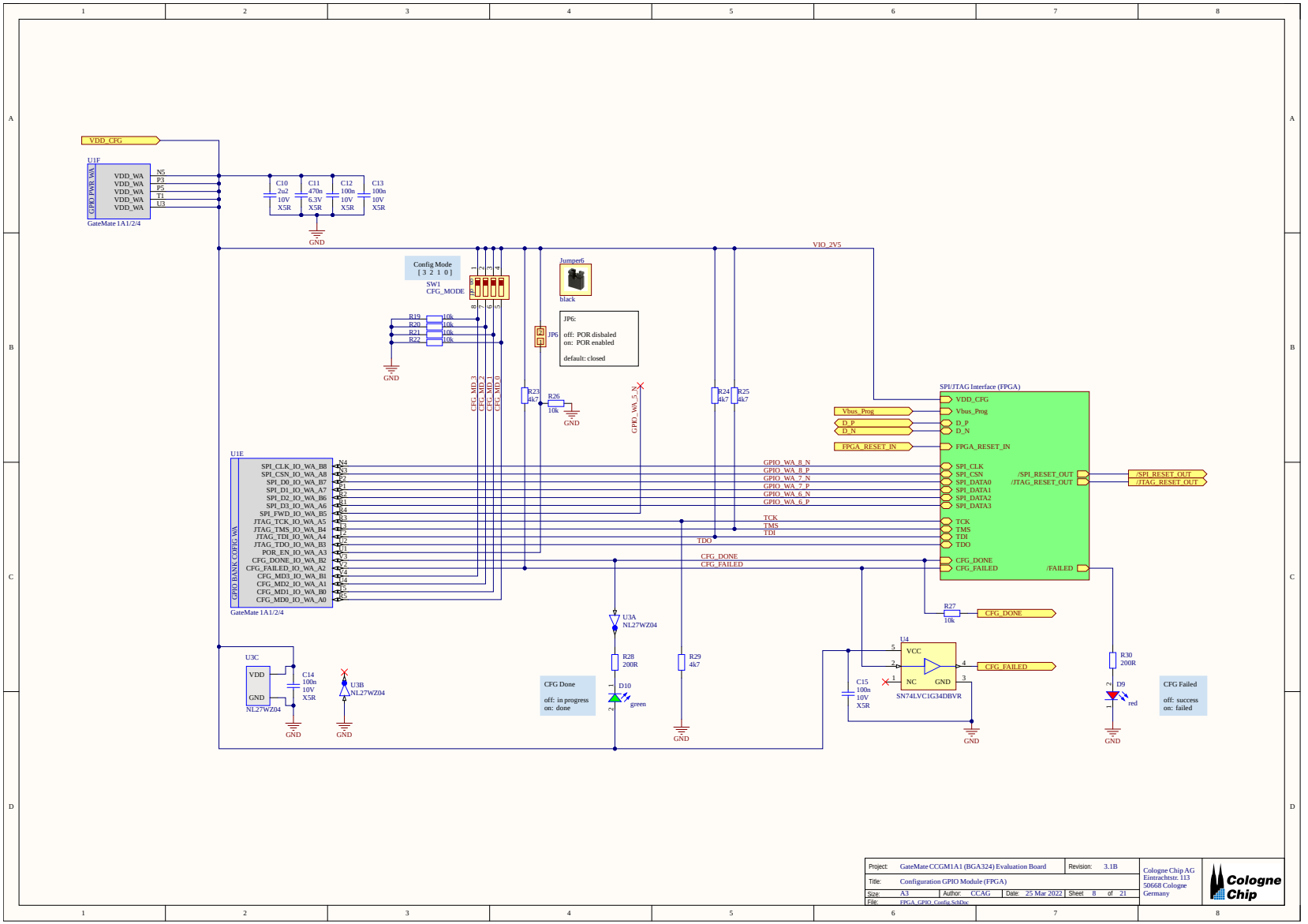
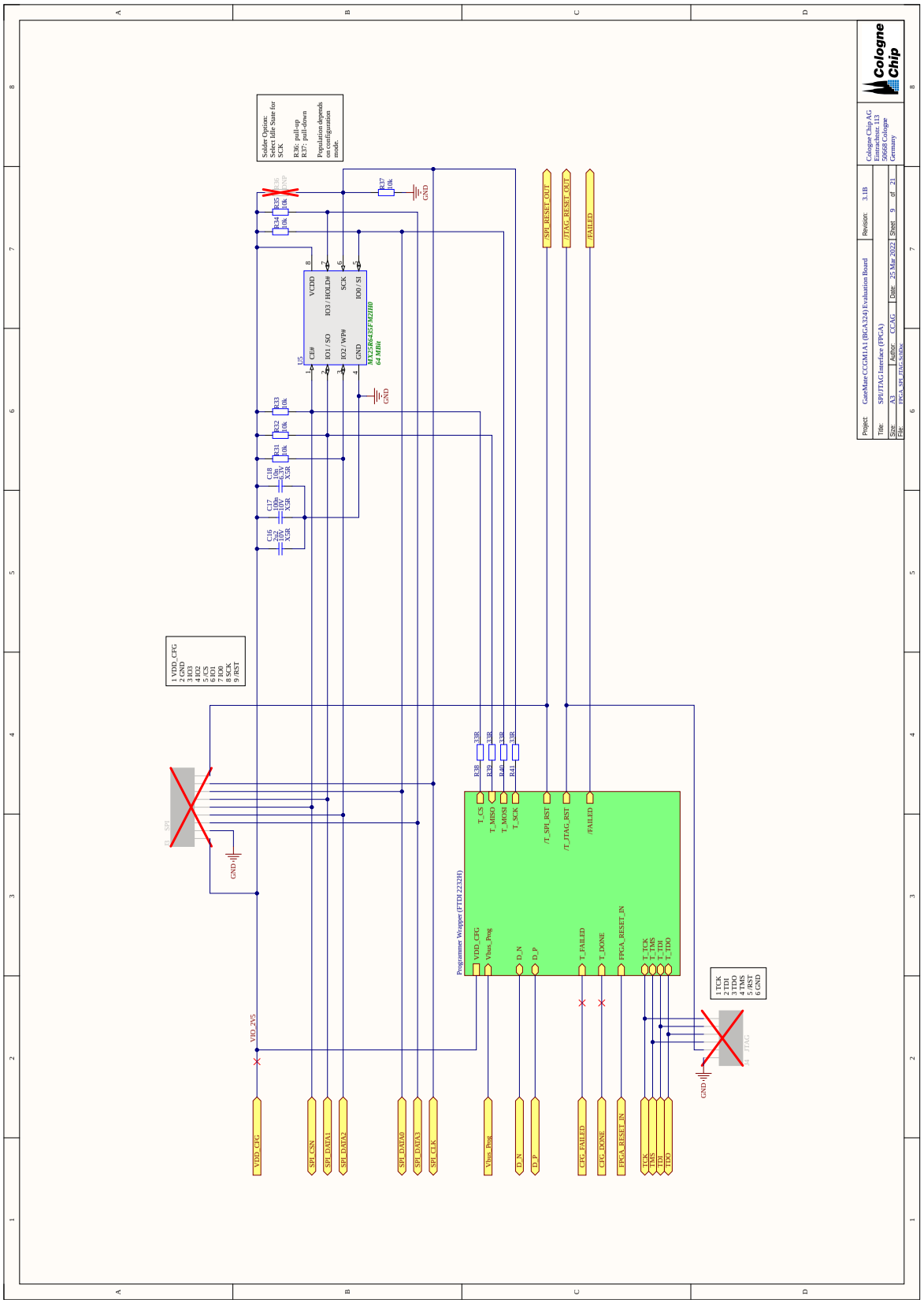
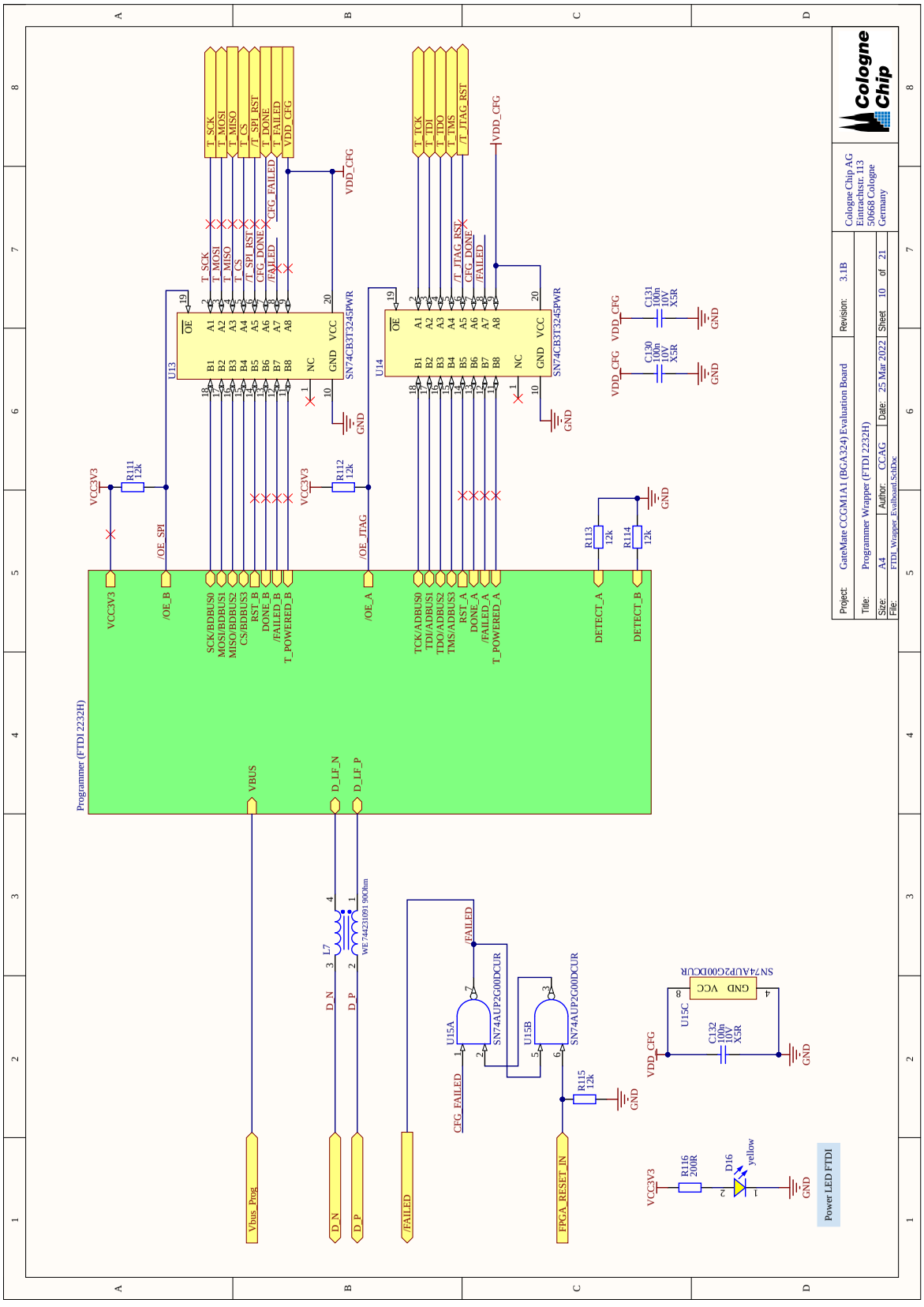
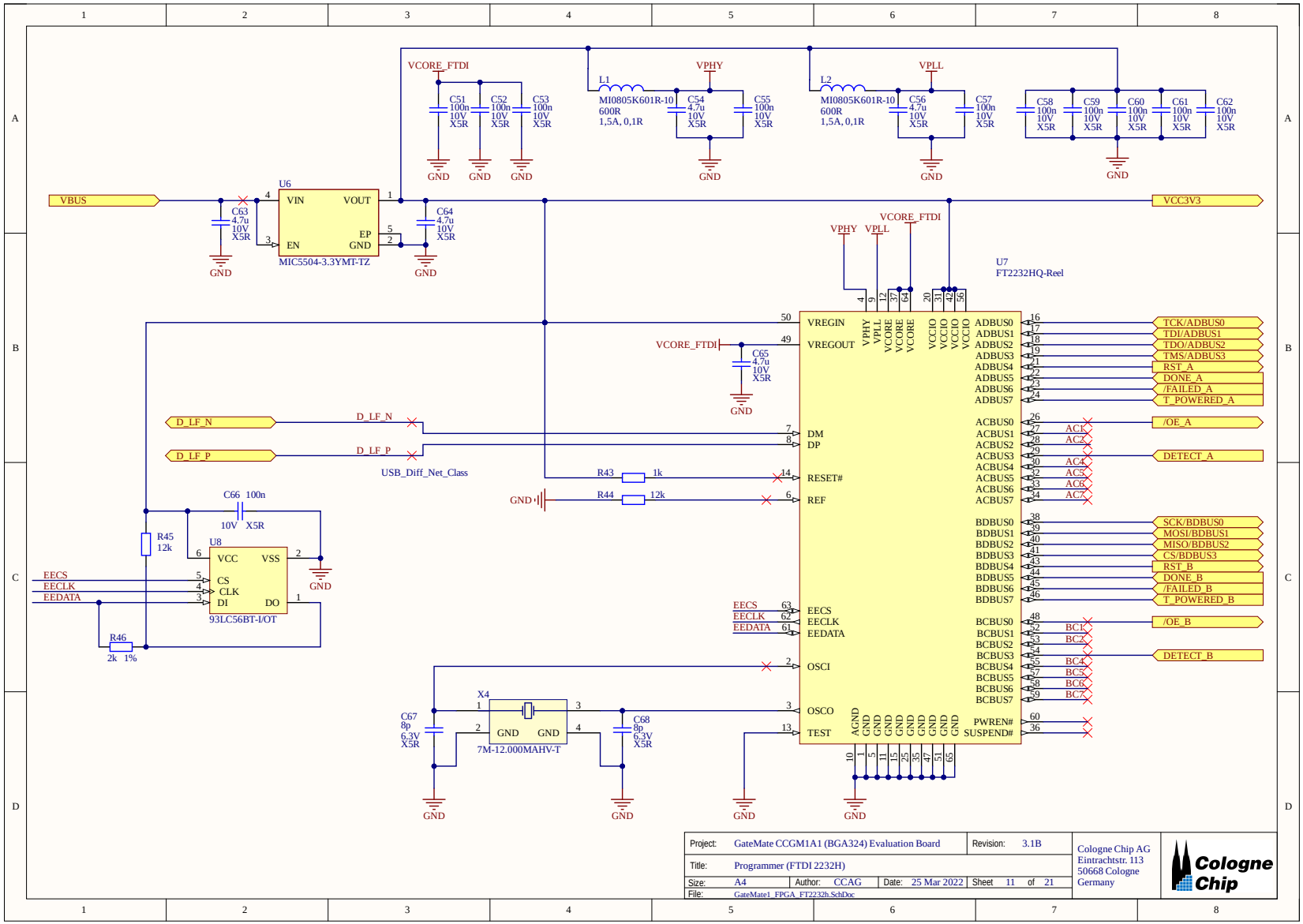
Germany

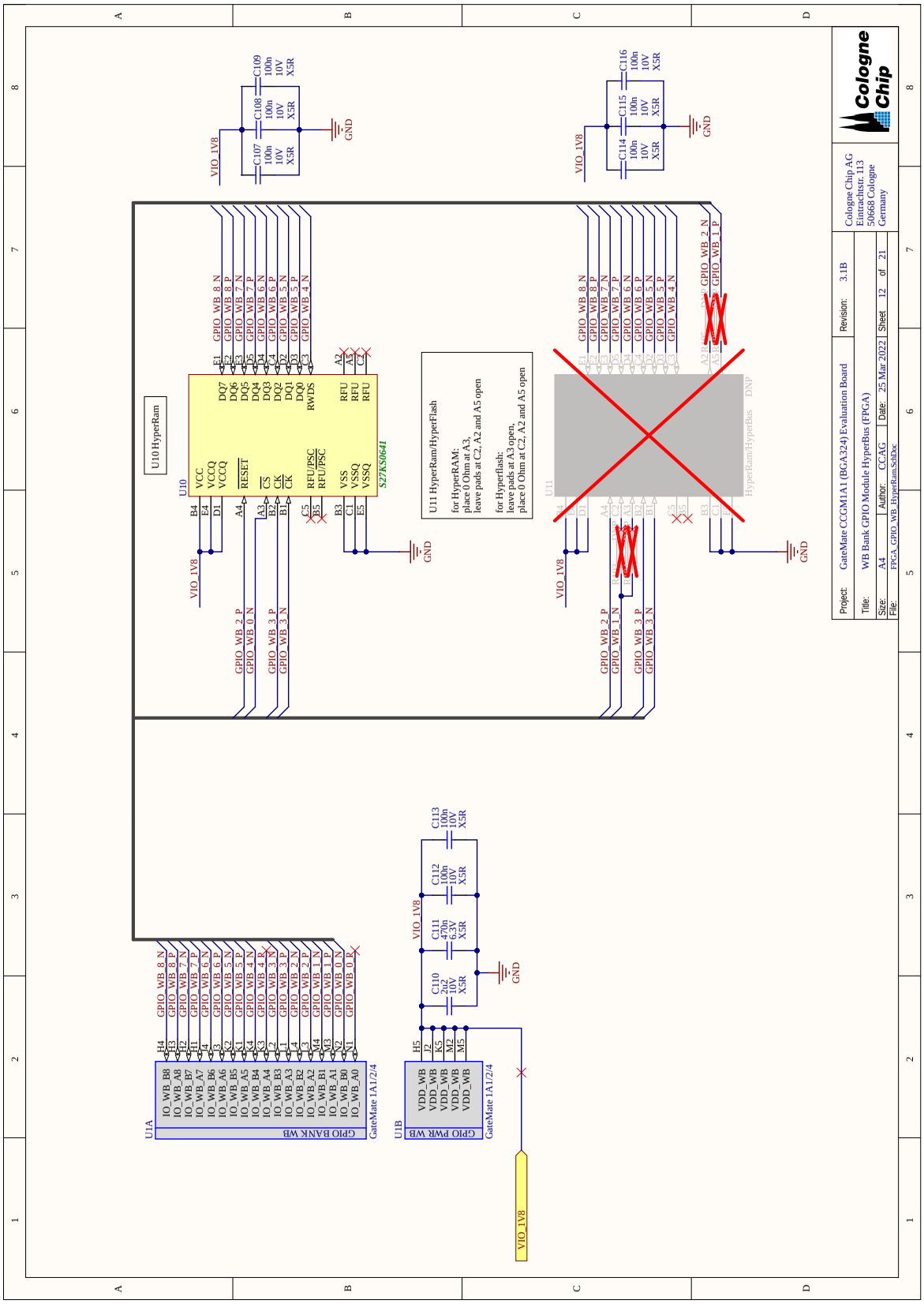

APP_RESET_IN
APP_SOUTH_CFG_DONE
APP_SOUTH_CFG_FAILED
APP_SOUTH_CLK2_OUT
APP_RESET_OUT
APP_SOUTH_CLK3_OUT
GPIO_Diff_Net_Class
U1O
GPIO BANK SB
IO_SB_B8 N15 GPIO_SB_8_N
IO_SB_A8 N14 GPIO_SB_8_P
IO_SB_B7 P13 GPIO_SB_7_N
IO_SB_A7 P12 GPIO_SB_7_P
IO_SB_B6 P15 GPIO_SB_6_N
IO_SB_A6 P14 GPIO_SB_6_P
IO_SB_B5 R14 GPIO_SB_5_N
IO_SB_A5 R13 GPIO_SB_5_P
IO_SB_B4 R11 GPIO_SB_4_N
IO_SB_A4 P11 GPIO_SB_4_P
GateMate 1A1/2/4
U1X
1A1/1A2/1A4
UNEQUAL PINS 1A1/2/4
IO_SB_A1/IO_SB_A1/SER_TX_P2 R17 GPIO_SB_1_P
IO_SB_B1/IO_SB_B1/SER_TX_N2 R18 GPIO_SB_1_N
VDD_SB/VDD_SB/SER_RTERM2 T18
IO_SB_A0/IO_SB_A0/SER_RX_P2 U17 GPIO_SB_0_P
IO_SB_B0/IO_SB_B0/SER_RX_N2 U18 GPIO_SB_0_N
IO_SB_A3/IO_SB_A3/SER_TX_P3 M17 GPIO_SB_3_P
IO_SB_B3/IO_SB_B3/SER_TX_N3 M18 GPIO_SB_3_N
VDD_SB/VDD_SB/SER_RTERM3 N18
IO_SB_A2/IO_SB_A2/SER_RX_P3 P17 GPIO_SB_2_P
IO_SB_B2/IO_SB_B2/SER_RX_N3 P18 GPIO_SB_2_N
GateMate 1A1/2/4
R70 0R
R71 0R
VIO_2V5
U1P
GPIO PWR SB
VDD_SB N11
VDD_SB N13
VDD_SB R15
GateMate 1A1/2/4
C84 2u2 10V X5R
C85 470n 6.3V X5R
C86 100n 10V X5R
C87 100n 10V X5R
GND
VDD_APP
VIO_3V3
J10
WCON 2320T
GPIO_SB_0_N GPIO_SB_0_P
GPIO_SB_1_N GPIO_SB_1_P
GPIO_SB_2_N GPIO_SB_2_P
GPIO_SB_3_N GPIO_SB_3_P
GPIO_SB_4_N GPIO_SB_4_P
GPIO_SB_5_N GPIO_SB_5_P
GPIO_SB_6_N GPIO_SB_6_P
GPIO_SB_7_N GPIO_SB_7_P
GPIO_SB_8_N GPIO_SB_8_P
R66 0R
46 GND
44 CFGD
42 RSTin
40 GND
38 CLK2out
36 GND
34 B[0]
32 B[1]
30 B[2]
28 GND
26 B[3]
24 B[4]
22 B[5]
20 GND
18 B[6]
16 B[7]
14 B[8]
12 GND
10 Vapp
8 GND
6 VIOin
4 VIOout
2 GND
45 GND
43 CFGF
41 RSTout
39 GND
37 CLK3out
35 GND
33 A[0]
31 A[1]
29 A[2]
27 GND
25 A[3]
23 A[4]
21 A[5] / Clock3
19 GND
17 A[6] / Clock2
15 A[7] / Clock1
13 A[8] / Clock0
11 GND
9 Vapp
7 GND
5 VIOin
3 VIOout
1 GND
IO_SB_A8 = Clock0
IO_SB_A7 = Clock1
IO_SB_A6 = Clock2
IO_SB_A5 = Clock3
CLOCK_0
CLOCK_1
CLOCK_2
CLOCK_3
Project: GateMate CCGM1A1 (BGA324) Evaluation Board
Revision: 3.1B
Title: SB Bank GPIO Module (FPGA)
Size: A4
Author: CCAG
Date: 25 Mar 2022
Sheet 7 of 21
File: FPGA_GPIO_SB.SchDoc
Cologne Chip AG
Eintrachtstr. 113
50668 Cologne
Germany
Cologne Chip

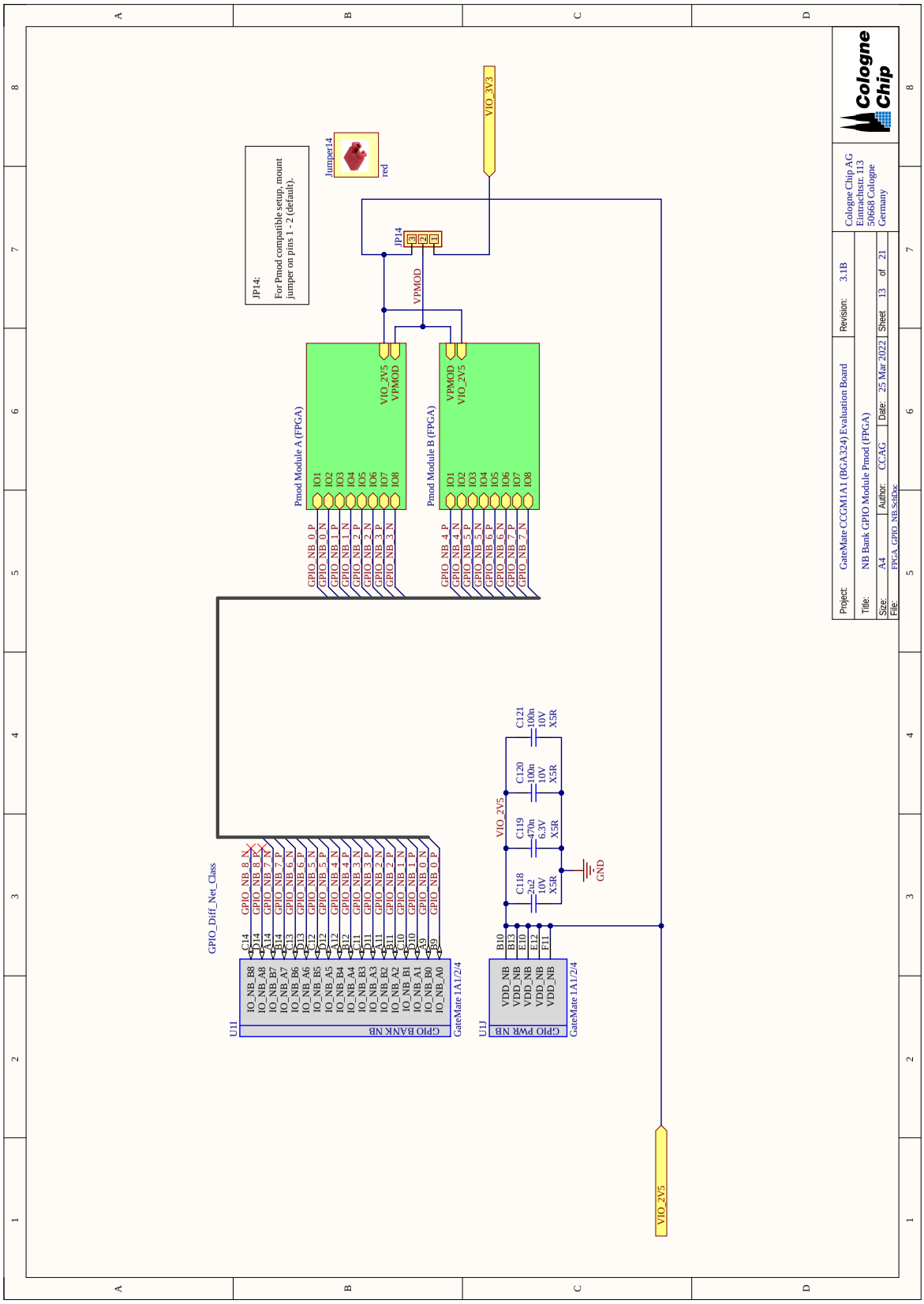

VDD_CFG
U1F
GPIO_PWR_WA
VDD_WA
VDD_WA
VDD_WA
VDD_WA
VDD_WA
N5
P3
P5
T1
U3
GateMate 1A1/2/4
C10 2u2 10V X5R
C11 470n 6.3V X5R
C12 100n 10V X5R
C13 100n 10V X5R
GND
VIO_2V5
Config Mode
[3 2 1 0]
SW1
CFG_MODE
Jumper6
black
JP6:
off: POR disbaled
on: POR enabled
default: closed
JP6
R19 10k
R20 10k
R21 10k
R22 10k
R23 4k7
R24 4k7
R25 4k7
R26 10k
CFG_MD3
CFG_MD2
CFG_MD1
CFG_MD0
GPIO_WA_5_N
U1E
GPIO_BANK_CORE_WA
SPI_CLK_IO_WA_B8
SPI_CSN_IO_WA_A8
SPI_D0_IO_WA_B7
SPI_D1_IO_WA_A7
SPI_D2_IO_WA_B6
SPI_D3_IO_WA_A6
SPI_FWD_IO_WA_B5
JTAG_TCK_IO_WA_A5
JTAG_TMS_IO_WA_B4
JTAG_TDI_IO_WA_A4
JTAG_TDO_IO_WA_B3
POR_EN_IO_WA_A3
CFG_DONE_IO_WA_B2
CFG_FAILED_IO_WA_A2
CFG_MD3_IO_WA_B1
CFG_MD2_IO_WA_A1
CFG_MD1_IO_WA_B0
CFG_MD0_IO_WA_A0
GateMate 1A1/2/4
SPI/JTAG Interface (FPGA)
VDD_CFG
Vbus_Prog
D_P
D_N
FPGA_RESET_IN
SPI_CLK
SPI_CSN
SPI_DATA0
SPI_DATA1
SPI_DATA2
SPI_DATA3
/SPI_RESET_OUT
/JTAG_RESET_OUT
TCK
TMS
TDI
TDO
CFG_DONE
CFG_FAILED
/FAILED
GPIO_WA_8_N
GPIO_WA_8_P
GPIO_WA_7_N
GPIO_WA_7_P
GPIO_WA_6_N
GPIO_WA_6_P
R27 10k
U3A
NL27WZ04
R28 200R
R29 4k7
U3C
VDD
GND
NL27WZ04
C14 100n 10V X5R
U3B
NL27WZ04
CFG Done
off: in progress
on: done
D10
green
U4
VCC
NC
GND
SN74LVC1G34DBVR
C15 100n 10V X5R
R30 200R
D9
red
CFG Failed
off: success
on: failed
Project: GateMate CCGM1A1 (BGA324) Evaluation Board
Revision: 3.1B
Title: Configuration GPIO Module (FPGA)
Size: A3
Author: CCAG
Date: 25 Mar 2022
Sheet 8 of 21
File: FPGA_GPIO_Config.SchDoc
Cologne Chip AG
Eintrachtstr. 113
50668 Cologne
Germany
Cologne Chip

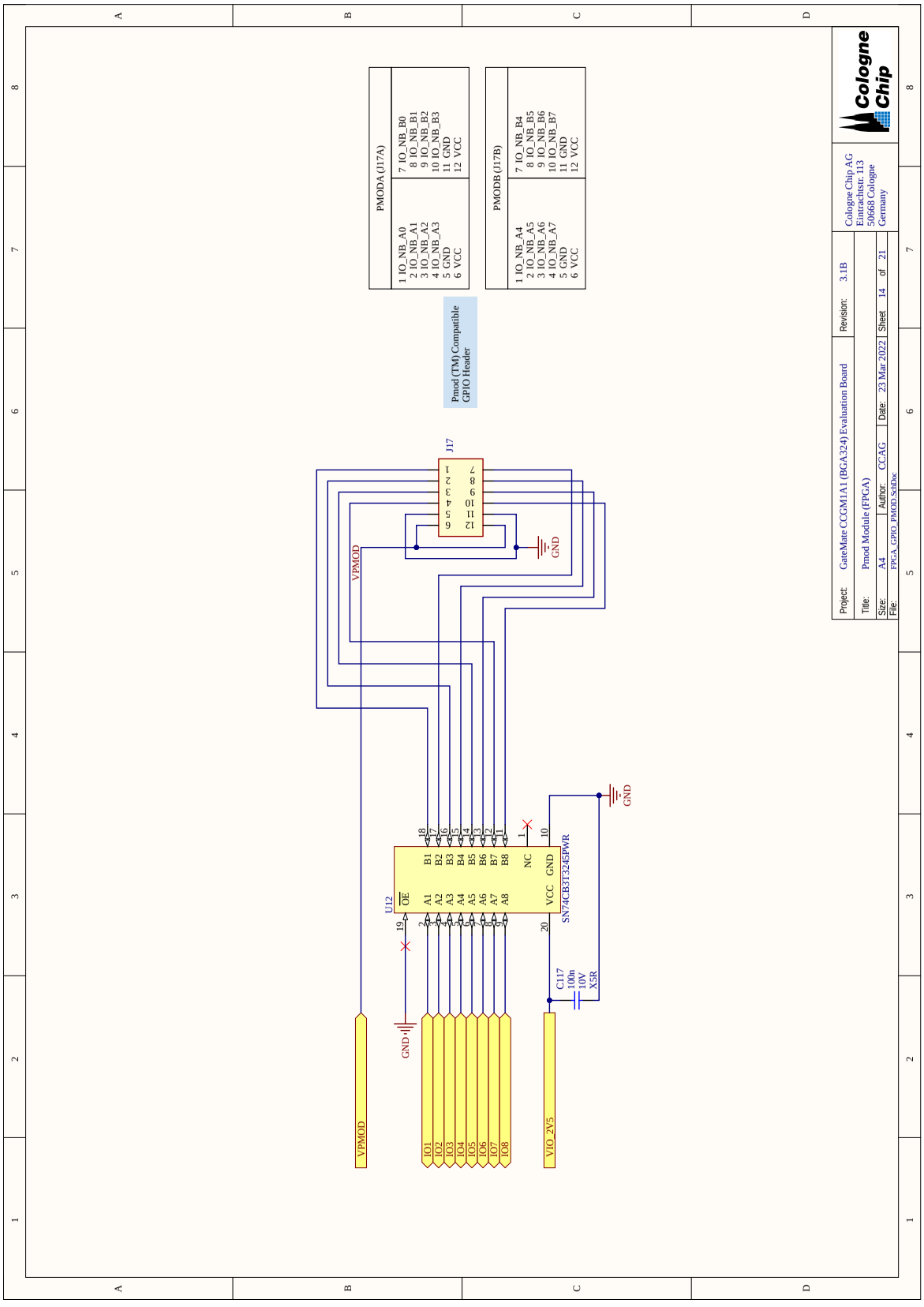

Project: GateMate:CCGM1A1 (BGA324) Evaluation Board
Revision: 3.1B
Title: SPI/JTAG Interface (FPGA)
Size: A3
Author: CCAG
Date: 25 Mar 2022
Sheet 9 of 21
File: FPGA_SPI_JTAG.SchDoc
Cologne Chip AG
Einrichstrasse 113
50668 Cologne
Germany
Solder Option:
Select Idle State for SCK
R36: pull-up
R37: pull-down
Population depends on configuration mode.
U5
MX25R6435FM2IH0
64 MBit
VCDD
IO3 / HOLD#
SCK
IO0 / SI
CE#
IO1 / SO
IO2 / WP#
GND
VDD_CFG
Vbus_Prog
D_N
D_P
T_FAILED
T_DONE
FPGA_RESET_IN
T_TCK
T_TMS
T_TDI
T_TDO
T_CS
T_MISO
T_MOSI
T_SCK
/T_SPI_RST
/T_JTAG_RST
/FAILED
Programmer Wrapper (FT2H 2232H)
/SPI_RESET_OUT
/JTAG_RESET_OUT
/FAILED
VIO_2V5
GND
SPI_CSN
SPI_DATA1
SPI_DATA2
SPI_DATA0
SPI_DATA3
SPI_CLK
CFG_FAILED
CFG_DONE
TCK
TMS
TDI
TDO
1 VDD_CFG
2 GND
3 IO3
4 IO2
5 /CS
6 IO1
7 IO0
8 SCK
9 /RST
1 TCK
2 TDI
3 TDO
4 TMS
5 /RST
6 GND

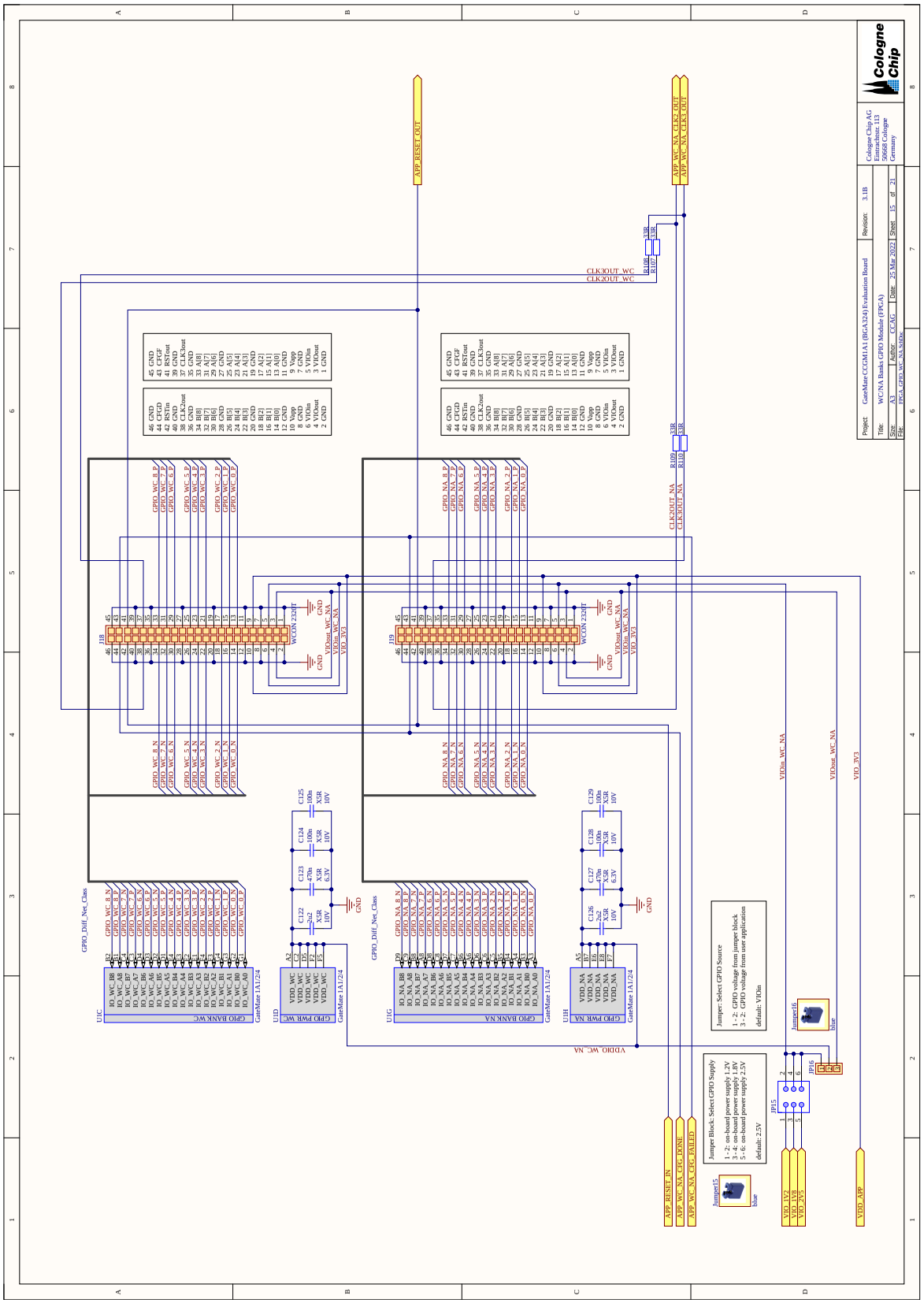

Programmer (FTDI 2232H)
SN74CB3T3245PWR
U13
U14
U15A
U15B
U15C
SN74AUP2G00DCUR
L7
WE 744231091 900hm
R111 12k
R112 12k
R113 12k
R114 12k
R115 12k
R116 200R
C130 100n 10V X5R
C131 100n 10V X5R
C132 100n 10V X5R
D16 yellow
VCC3V3
VDD_CFG
GND
/OE_SPI
/OE_JTAG
/OE_B
/OE_A
VBUS
D_LF_N
D_LF_P
D_N
D_P
/FAILED
CFG_FAILED
FPGA_RESET_IN
Vbus_Prog
Power LED FTDI
T_SCK
T_MOSI
T_MISO
T_CS
/T_SPI_RST
T_DONE
T_FAILED
T_TCK
T_TDI
T_TDO
T_TMS
/T_JTAG_RST
CFG_DONE
SCK/BDBUS0
MOSI/BDBUS1
MISO/BDBUS2
CS/BDBUS3
RST_B
DONE_B
/FAILED_B
T_POWERED_B
TCK/ADBUS0
TDI/ADBUS1
TDO/ADBUS2
TMS/ADBUS3
RST_A
DONE_A
/FAILED_A
T_POWERED_A
DETECT_A
DETECT_B
Project: GateMate CCGM1A1 (BGA324) Evaluation Board
Revision: 3.1B
Title: Programmer Wrapper (FTDI 2232H)
Size: A4
Author: CCAG
Date: 25 Mar 2022
Sheet 10 of 21
File: FTDI_Wrapper_Evalboard.SchDoc
Cologne Chip AG
Eintrachtstr. 113
50668 Cologne
Germany

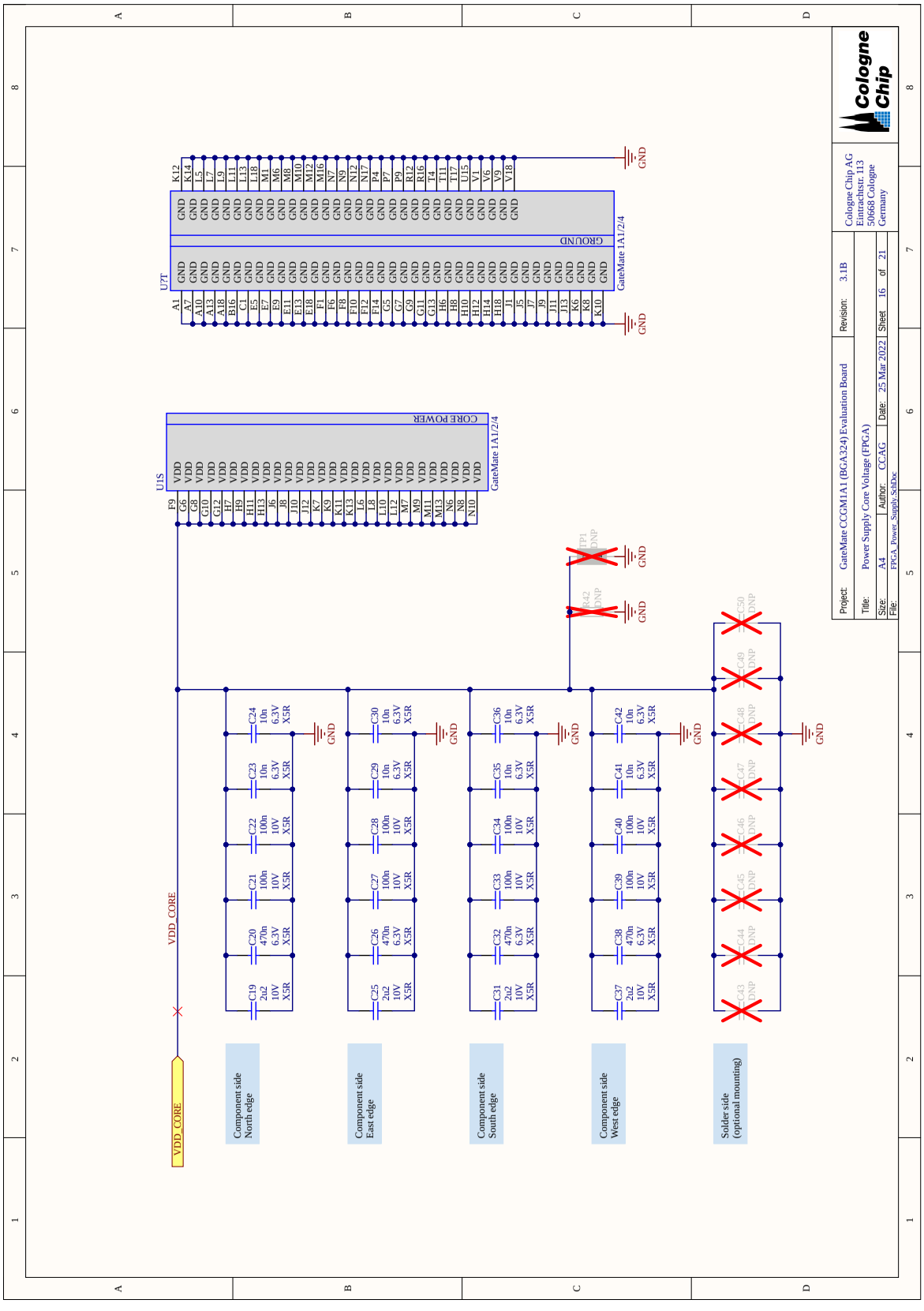

VCORE_FTDI
VPHY
VPLL
L1
MI0805K601R-10
600R
1,5A, 0,1R
L2
MI0805K601R-10
600R
1,5A, 0,1R
C51 100n 10V X5R
C52 100n 10V X5R
C53 100n 10V X5R
C54 4.7u 10V X5R
C55 100n 10V X5R
C56 4.7u 10V X5R
C57 100n 10V X5R
C58 100n 10V X5R
C59 100n 10V X5R
C60 100n 10V X5R
C61 100n 10V X5R
C62 100n 10V X5R
GND
U6
VIN
VOUT
EP
EN
GND
MIC5504-3.3YMT-TZ
VBUS
VCC3V3
C63 4.7u 10V X5R
C64 4.7u 10V X5R
U7
FT2232HQ-Reel
VREGIN
VREGOUT
C65 4.7u 10V X5R
D_LF_N
D_LF_P
USB_Diff_Net_Class
DM
DP
RESET#
REF
R43 1k
R44 12k
C66 100n 10V X5R
R45 12k
R46 2k 1%
U8
VCC
VSS
CS
CLK
DI
DO
93LC56BT-I/OT
EECS
EECLK
EEDATA
X4
7M-12.000MAHV-T
C67 8p 6.3V X5R
C68 8p 6.3V X5R
OSCI
OSCO
TEST
PWREN#
SUSPEND#
ADBUS0
ADBUS1
ADBUS2
ADBUS3
ADBUS4
ADBUS5
ADBUS6
ADBUS7
TCK/ADBUS0
TDI/ADBUS1
TDO/ADBUS2
TMS/ADBUS3
RST_A
DONE_A
/FAILED_A
T_POWERED_A
ACBUS0
ACBUS1
ACBUS2
ACBUS3
ACBUS4
ACBUS5
ACBUS6
ACBUS7
/OE_A
DETECT_A
BDBUS0
BDBUS1
BDBUS2
BDBUS3
BDBUS4
BDBUS5
BDBUS6
BDBUS7
SCK/BDBUS0
MOSI/BDBUS1
MISO/BDBUS2
CS/BDBUS3
RST_B
DONE_B
/FAILED_B
T_POWERED_B
BCBUS0
BCBUS1
BCBUS2
BCBUS3
BCBUS4
BCBUS5
BCBUS6
BCBUS7
/OE_B
DETECT_B
Project: GateMate CCGM1A1 (BGA324) Evaluation Board
Revision: 3.1B
Title: Programmer (FTDI 2232H)
Size: A4
Author: CCAG
Date: 25 Mar 2022
Sheet 11 of 21
File: GateMate1_FPGA_FT2232h.SchDoc
Cologne Chip AG
Eintrachtstr. 113
50668 Cologne
Germany

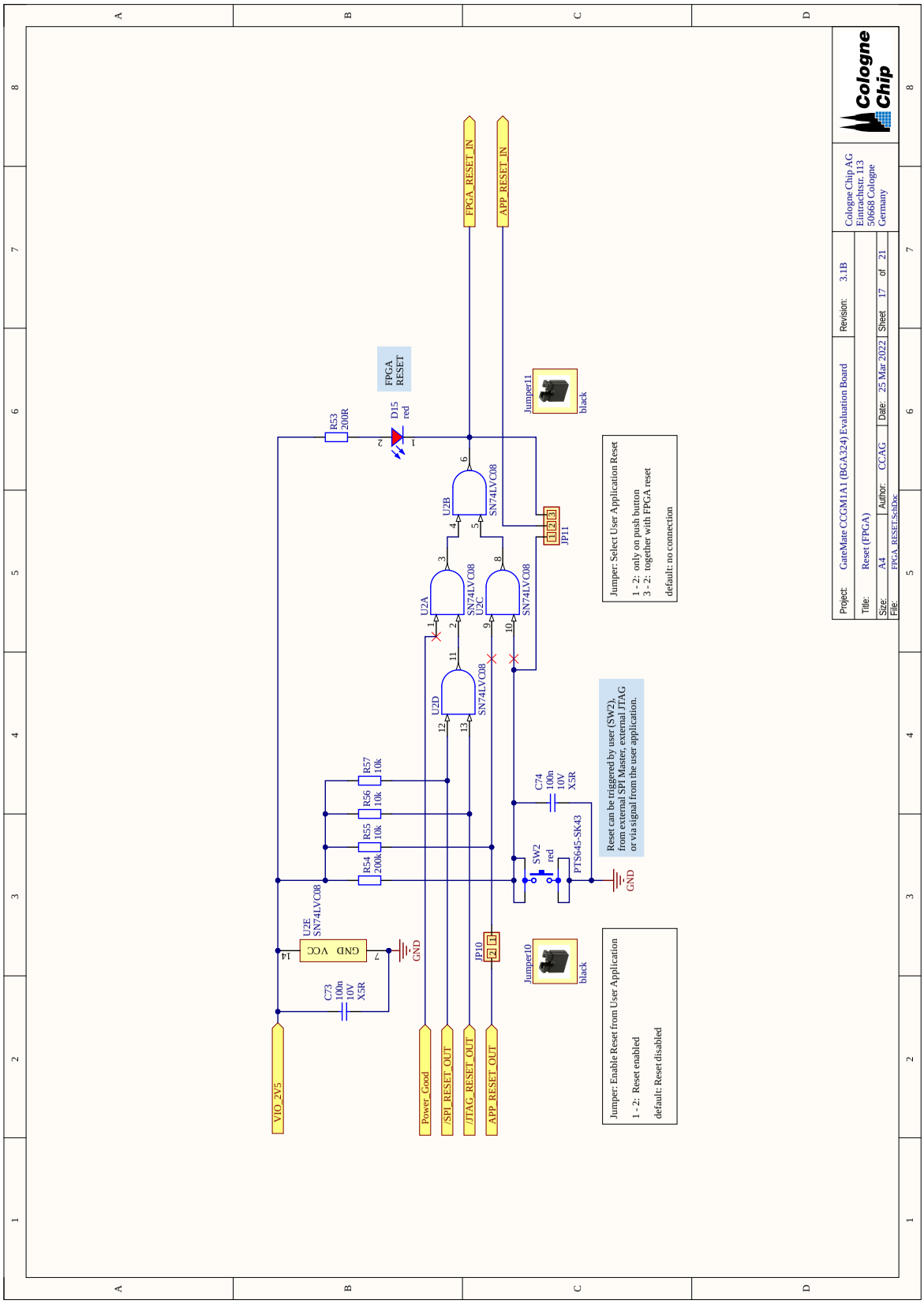

U10 HyperRam
U11 HyperRam/HyperFlash
for HyperRAM:
place 0 Ohm at A3,
leave pads at C2, A2 and A5 open
for Hyperflash:
leave pads at A3 open,
place 0 Ohm at C2, A2 and A5 open
S27KS0641
HyperRam/HyperBus
DNP
GateMate 1A1/2/4
GPIO BANK WB
GPIO PWR WB
VIO_1V8
GND
Project: GateMate CCGM1A1 (BGA324) Evaluation Board
Revision: 3.1B
Title: WB Bank GPIO Module HyperBus (FPGA)
Size: A4
Author: CCAG
Date: 25 Mar 2022
Sheet 12 of 21
File: FPGA_GPIO_WB_HyperRam.SchDoc
Cologne Chip AG
Eintrachtstr. 113
50668 Cologne
Germany


JP14:
For Pmod compatible setup, mount jumper on pins 1 - 2 (default).
Jumper14
red
VIO_3V3
JP14
VPMOD
Pmod Module A (FPGA)
Pmod Module B (FPGA)
VIO_2V5
VPMOD
GPIO_NB_0_P
GPIO_NB_0_N
GPIO_NB_1_P
GPIO_NB_1_N
GPIO_NB_2_P
GPIO_NB_2_N
GPIO_NB_3_P
GPIO_NB_3_N
GPIO_NB_4_P
GPIO_NB_4_N
GPIO_NB_5_P
GPIO_NB_5_N
GPIO_NB_6_P
GPIO_NB_6_N
GPIO_NB_7_P
GPIO_NB_7_N
GPIO_Diff_Net_Class
U1I
GPIO BANK NB
GateMate 1A1/2/4
U1J
GPIO PWR NB
C118 2n2 10V X5R
C119 470n 6.3V X5R
C120 100n 10V X5R
C121 100n 10V X5R
GND
Cologne Chip AG
Eintrachtstr. 113
50668 Cologne
Germany
Project: GateMate CCGM1A1 (BGA324) Evaluation Board
Revision: 3.1B
Title: NB Bank GPIO Module Pmod (FPGA)
Size: A4
Author: CCAG
Date: 25 Mar 2022
Sheet 13 of 21
File: FPGA_GPIO_NB.SchDoc


PMODA (J17A)
1 IO_NB_A0
2 IO_NB_A1
3 IO_NB_A2
4 IO_NB_A3
5 GND
6 VCC
7 IO_NB_B0
8 IO_NB_B1
9 IO_NB_B2
10 IO_NB_B3
11 GND
12 VCC
PMODB (J17B)
1 IO_NB_A4
2 IO_NB_A5
3 IO_NB_A6
4 IO_NB_A7
5 GND
6 VCC
7 IO_NB_B4
8 IO_NB_B5
9 IO_NB_B6
10 IO_NB_B7
11 GND
12 VCC
Pmod (TM) Compatible GPIO Header
J17
VPMOD
GND
U12
SN74CB3T3245PWR
C117
100n
10V
X5R
VIO_2V5
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
Project: GateMate CCGM1A1 (BGA324) Evaluation Board
Revision: 3.1B
Title: Pmod Module (FPGA)
Size: A4
Author: CCAG
Date: 23 Mar 2022
Sheet 14 of 21
File: FPGA_GPIO_PMOD.Schdoc
Cologne Chip AG
Eintrachtstr. 113
50668 Cologne
Germany


Cologne Chip
Project: GateMate CCGM1A1 (BGA324) Evaluation Board
Revision: 3.1B
Title: WC/NA Banks GPIO Module (FPGA)
Author: CCAG
Date: 25 Mar 2022
Sheet: 15 of 21
File: FPGA_GPIO_WC_NA.SchDoc
Cologne Chip AG
Einsteinchstr. 113
59368 Cologne
Germany
APP_RESET_OUT
APP_WC_NA_CLK2_OUT
APP_WC_NA_CLK3_OUT
CLK3OUT_WC
CLK2OUT_WC
CLK2OUT_NA
CLK3OUT_NA
GPIO_WC_8_P
GPIO_WC_7_P
GPIO_WC_6_P
GPIO_WC_5_P
GPIO_WC_4_P
GPIO_WC_3_P
GPIO_WC_2_P
GPIO_WC_1_P
GPIO_WC_0_P
GPIO_NA_8_P
GPIO_NA_7_P
GPIO_NA_6_P
GPIO_NA_5_P
GPIO_NA_4_P
GPIO_NA_3_P
GPIO_NA_2_P
GPIO_NA_1_P
GPIO_NA_0_P
WCON-232HT
VIOin_WC_NA
VIOout_WC_NA
VIO_3V3
VDDIO_WC_NA
VDD_APP
Jumper: Select GPIO Source
1 -2: GPIO voltage from jumper block
3 -2: GPIO voltage from user application
default: VIOin
Jumper Block: Select GPIO Supply
1 -2: on-board power supply 1.2V
3 -4: on-board power supply 1.8V
5 -6: on-board power supply 2.5V
default: 2.5V
APP_RESET_IN
APP_WC_NA_CFG_DONE
APP_WC_NA_CFG_FAILED


U7T
GROUND
GateMate 1A1/2/4
U1S
CORE POWER
GateMate 1A1/2/4
VDD_CORE
Component side North edge
Component side East edge
Component side South edge
Component side West edge
Solder side (optional mounting)
Project: GateMate CCGM1A1 (BGA324) Evaluation Board
Revision: 3.1B
Title: Power Supply Core Voltage (FPGA)
Size: A4
Author: CCAG
Date: 25 Mar 2022
Sheet 16 of 21
File: FPGA_Power_Supply.SchDoc
Cologne Chip AG
Eintrachtstr. 113
50668 Cologne
Germany


FPGA_RESET_IN
APP_RESET_IN
FPGA RESET
D15 red
R53 200R
Jumper11 black
U2B SN74LVC08
JP11
U2A SN74LVC08
U2C SN74LVC08
U2D SN74LVC08
U2E SN74LVC08
R57 10k
R56 10k
R55 10k
R54 200k
C74 100n 10V X5R
SW2 red
PTS645-SK43
GND
C73 100n 10V X5R
JP10
Jumper10 black
VIO_2V5
Power_Good
/SPI_RESET_OUT
/JTAG_RESET_OUT
APP_RESET_OUT
Jumper: Select User Application Reset
1 - 2: only on push button
3 - 2: together with FPGA reset
default: no connection
Reset can be triggered by user (SW2), from external SPI Master, external JTAG or via signal from the user application.
Jumper: Enable Reset from User Application
1 - 2: Reset enabled
default: Reset disabled
Project: GateMate CCGM1A1 (BGA324) Evaluation Board
Revision: 3.1B
Title: Reset (FPGA)
Size: A4
Author: CCAG
Date: 25 Mar 2022
Sheet 17 of 21
File: FPGA_RESET.SchDoc
Cologne Chip AG
Eintrachtstr. 113
50668 Cologne
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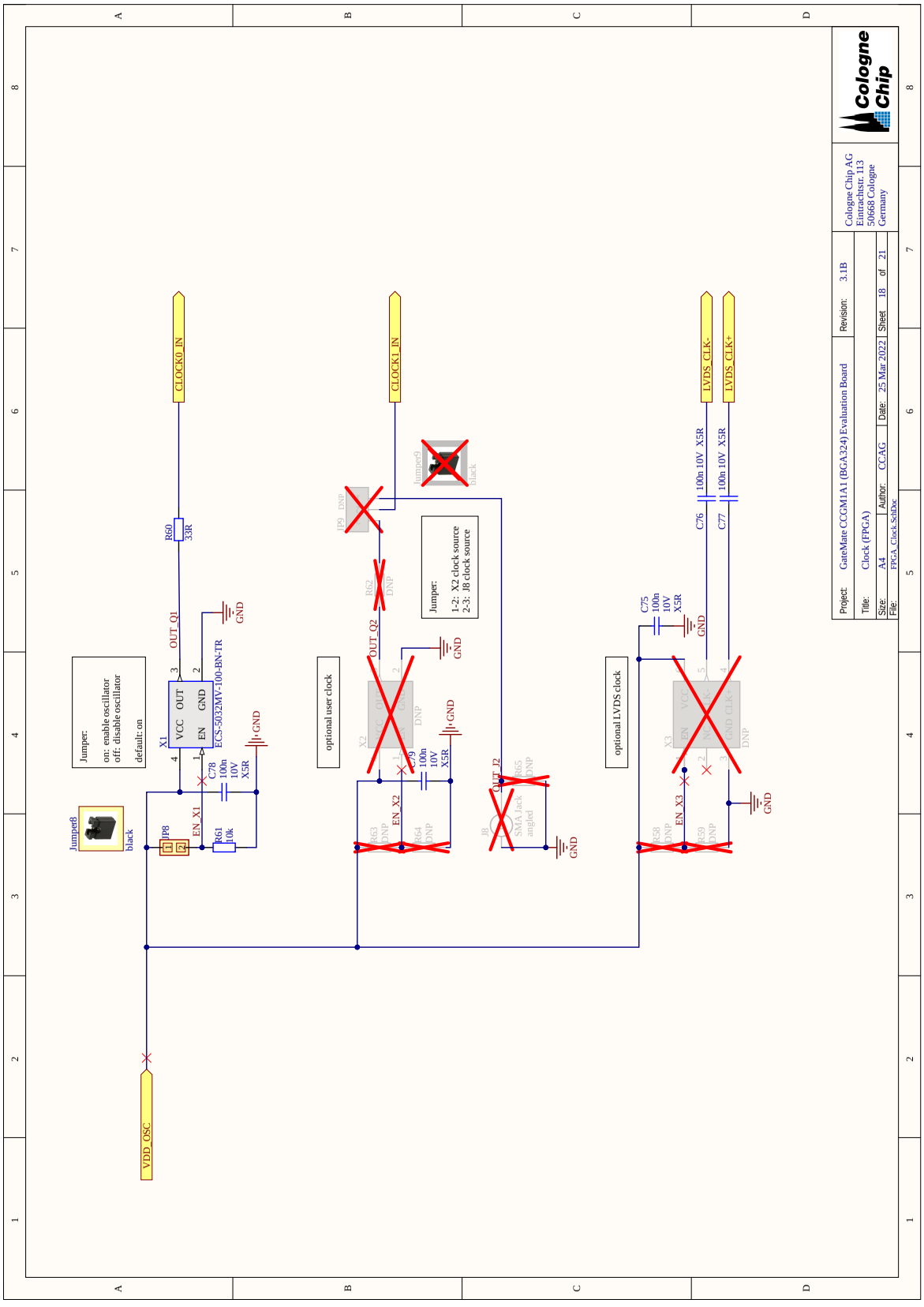
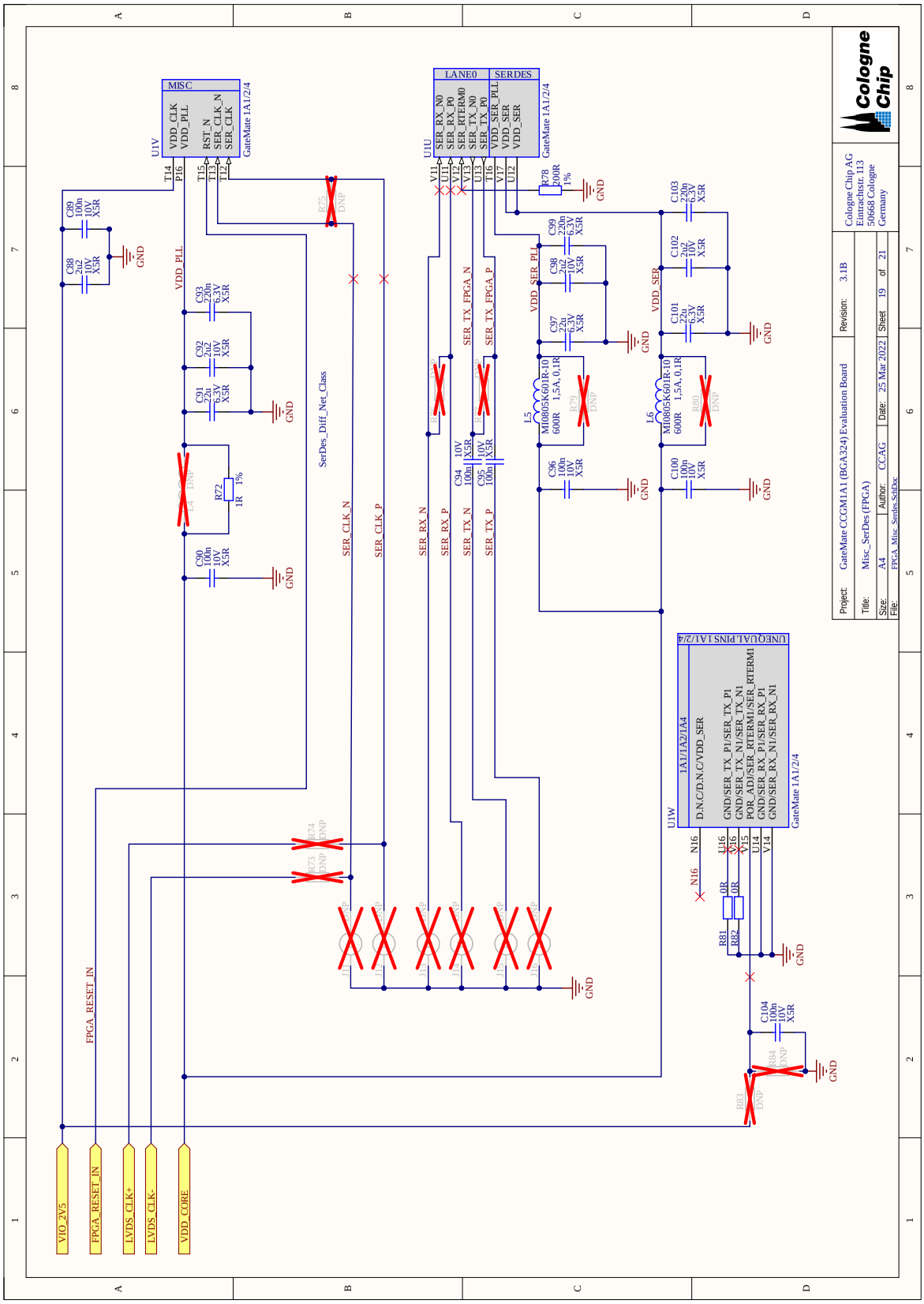
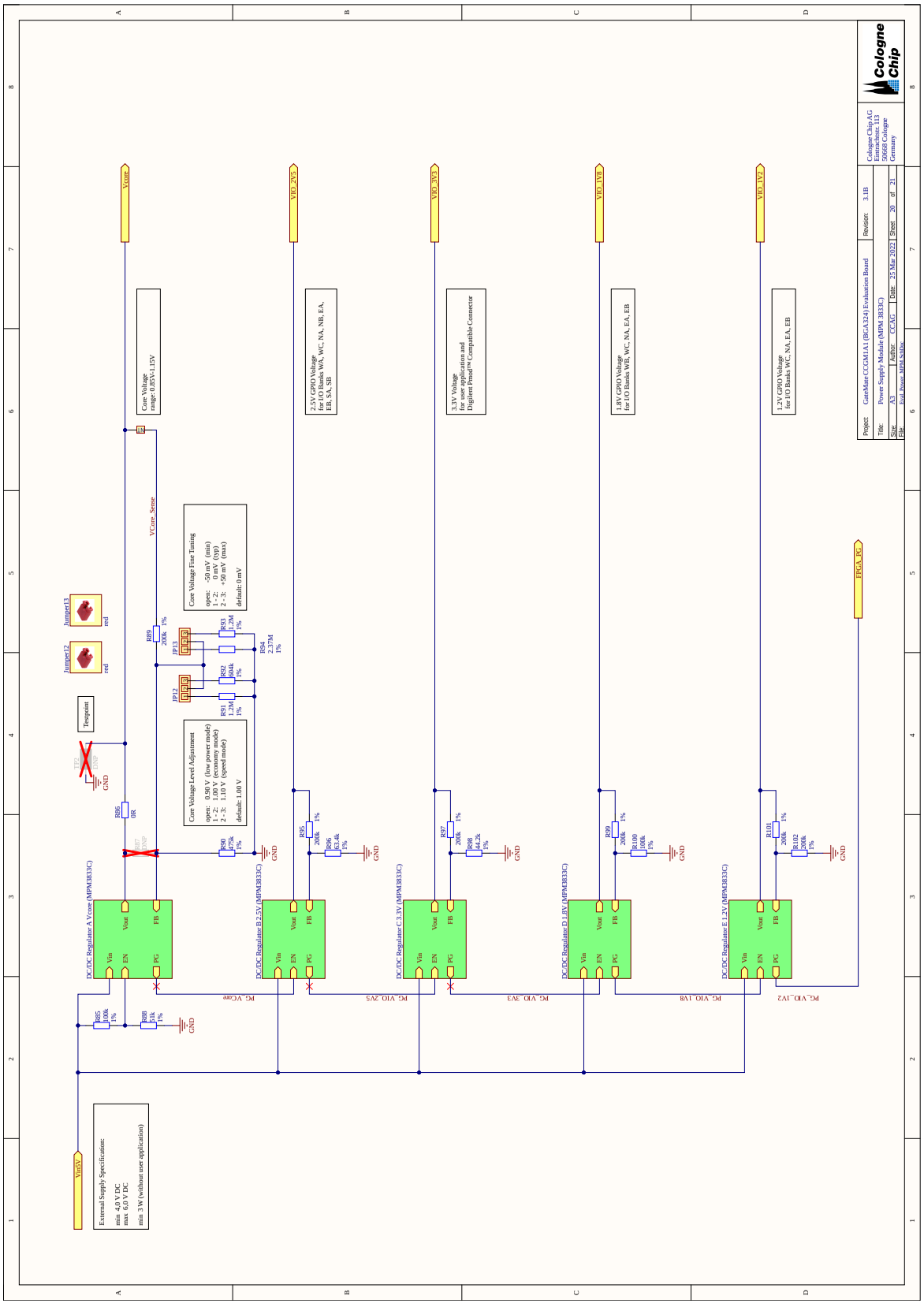
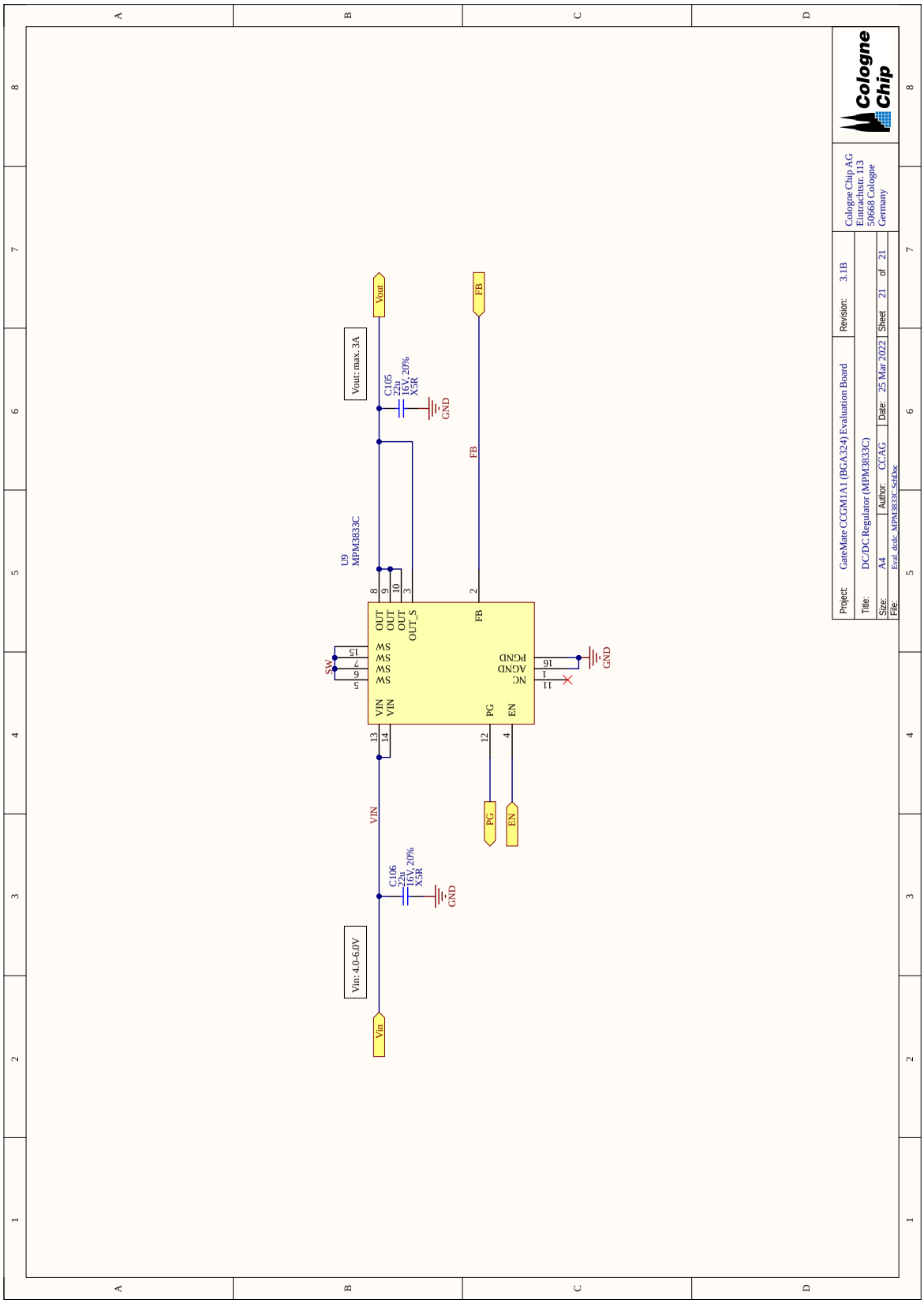

CLOCK0_IN
CLOCK1_IN
LVDS_CLK-
LVDS_CLK+
VDD_OSC
R60
33R
OUT_Q1
OUT_Q2
X1
ECS-5032MV-100-BN-TR
VCC OUT EN GND
C78
100n
10V
X5R
GND
JP8
EN_X1
R61
10k
Jumper6
black
Jumper:
on: enable oscillator
off: disable oscillator
default: on
optional user clock
JP3
DNP
R62
DNP
Jumper5
black
Jumper:
1-2: X2 clock source
2-3: J8 clock source
X2
R63
DNP
C79
100n
10V
X5R
R64
DNP
EN_X2
OUT_J2
J8
SMA Jack
angled
R65
DNP
optional LVDS clock
C75
100n
10V
X5R
C76
100n 10V X5R
C77
100n 10V X5R
X3
R58
DNP
R59
DNP
EN_X3
Project: GateMate CCGM1A1 (BGA324) Evaluation Board
Revision: 3.1B
Title: Clock (FPGA)
Size: A4
Author: CCAG
Date: 25 Mar 2022
Sheet 18 of 21
File: FPGA_Clock.SchDoc
Cologne Chip AG
Eintrachtstr. 113
50668 Cologne
Germany


MISC
VDD_CLK
VDD_PLL
RST_N
SER_CLK_N
SER_CLK
GateMate 1A1/2/4
LANE0
SERDES
SER_RX_N0
SER_RX_P0
SER_RTERM0
SER_TX_N0
SER_TX_P0
VDD_SER_PLL
VDD_SER
SER_TX_FPGA_N
SER_TX_FPGA_P
SerDes_Diff_Net_Class
SER_CLK_N
SER_CLK_P
SER_RX_N
SER_RX_P
SER_TX_N
SER_TX_P
FPGA_RESET_IN
VDD_PLL
VDD_SER_PLL
VDD_SER
UNEQUAL PINS 1A1/2/4
1A1/1A2/1A4
D.N.C/D.N.C/VDD_SER
GND/SER_TX_P1/SER_TX_P1
GND/SER_TX_N1/SER_TX_N1
POR_ADJ/SER_RTERM1/SER_RTERM1
GND/SER_RX_P1/SER_RX_P1
GND/SER_RX_N1/SER_RX_N1
VIO_2V5
FPGA_RESET_IN
LVDS_CLK+
LVDS_CLK-
VDD_CORE
Cologne Chip AG
Eintrachtstr. 113
50668 Cologne
Germany
Project: GateMate CCGM1A1 (BGA324) Evaluation Board
Revision: 3.1B
Title: Misc_SerDes (FPGA)
Size: A4
Author: CCAG
Date: 25 Mar 2022
Sheet 19 of 21
File: FPGA_Misc_SerdesSchDoc


Vcore
VIO_2V5
VIO_3V3
VIO_1V8
VIO_1V2
VCore_Sense
FPGA_PG
PG_VCore
PG_VIO_2V5
PG_VIO_3V3
PG_VIO_1V8
PG_VIO_1V2
DC/DC Regulator A Vcore (MPM3833C)
DC/DC Regulator B 2.5V (MPM3833C)
DC/DC Regulator C 3.3V (MPM3833C)
DC/DC Regulator D 1.8V (MPM3833C)
DC/DC Regulator E 1.2V (MPM3833C)
Core Voltage range: 0.85V-1.15V
2.5V GPIO Voltage for I/O Banks WA, WC, NA, NB, EA, EB, SA, SB
3.3V Voltage for user application and Digilent Pmod™ Compatible Connector
1.8V GPIO Voltage for I/O Banks WB, WC, NA, EA, EB
1.2V GPIO Voltage for I/O Banks WC, NA, EA, EB
Core Voltage Fine Tuning
Core Voltage Level Adjustment
External Supply Specification:
min 4.0 V DC
max 6.0 V DC
min 3 W (without user application)
Cologne Chip AG
Project: GateMate+CCGM1A1 [BGA324] Evaluation Board
Title: Power Supply Module (MPM 3833C)
Size: A3
Author: CCAG
Date: 25 Mar 2022
Sheet: 20 of 21
File: Eval_Board_MPM_3x3.kicad_sch
Revision: 3.1B


Project: GateMate CCGM1A1 (BGA324) Evaluation Board
Revision: 3.1B
Title: DC/DC Regulator (MPM3833C)
Size: A4
Author: CCAG
Date: 25 Mar 2022
Sheet 21 of 21
File: Eval_dcdc_MPM3833C.SchDoc
Cologne Chip AG
Eintrachtstr. 113
50668 Cologne
Germany
U9
MPM3833C
OUT
OUT
OUT
OUT_S
FB
SW
SW
SW
SW
PGND
AGND
NC
VIN
VIN
PG
EN
Vout
Vout: max. 3A
C105
22u
16V, 20%
X5R
GND
FB
Vin
Vin: 4.0-6.0V
C106
22u
16V, 20%
X5R
PG
EN
SW

Appendix C

Bill of Materials

Table C.1: *Bill of Materials (sorted by designator)*

Component	Specification	Designators	Count
10n	6.3V X5R	C18, C23, C24, C29, C30, C35, C36, C41, C42	9
4.7u	10V X5R	C54, C56, C63, C64, C65	5
8p	6.3V X5R	C67, C68	2
22u	6.3V X5R	C91, C97, C101	3
220n	6.3V X5R	C93, C99, C103	3
22u	16V, 20% X5R	C105A, C105B, C105C, C105D, C105E, C106A, C106B, C106C, C106D, C106E	10
2u2	10V X5R	C1, C5, C10, C16, C19, C25, C31, C37, C69, C71, C80, C84, C88, C92, C98, C102, C110, C118, C122, C126	20
470n	6.3V X5R	C2, C6, C11, C20, C26, C32, C38, C81, C85, C111, C119, C123, C127	13

Continued on next page

Table C.0: *Bill of Materials (sorted by designator)*

Continued from previous page

Component	Specification	Designators	Count
100n	10V X5R	C3, C4, C7, C8, C9, C12, C13, C14, C15, C17, C21, C22, C27, C28, C33, C34, C39, C40, C51, C52, C53, C55, C57, C58, C59, C60, C61, C62, C66, C70, C72, C73, C74, C75, C76, C77, C78, C79, C82, C83, C86, C87, C89, C90, C94, C95, C96, C100, C104, C107, C108, C109, C112, C113, C114, C115, C116, C117A, C117B, C120, C121, C124, C125, C128, C129, C130, C131, C132	68
WE-150 060 VS7 322	LED green	D1, D2, D3, D4, D5, D6, D7, D8, D10	9
SP3012-04UTG	TVS diode	D14	1
WE-150 060 RS7 322	LED red	D9, D15	2
WE-150 060 YS7 322	LED yellow	D11, D12, D13, D16	4
WE-61300311121	Header vertical 3 pins 2.54 mm	J6	1
Mini USB 2.0	Type B Receptacle	J5, J7	2
WE-613012243121	Box header vertical 2x6 pins 2.54 mm	J17A, J17B	2
WCON 2320T		J1, J2, J9, J10, J18, J19	6
WE-61300211121	Jumper 2 pins	JP4, JP6, JP8, JP10	4
WE-61300621121	Jumper 3x2 pins	JP3, JP15	2
WE-61300311121	Jumper 3 pins	JP5, JP7, JP11, JP12, JP13, JP14, JP16	7
MI0805K601R-10	600R 1,5A, 0,1R	L1, L2, L3, L5, L6	5
WE 744231091 90Ohm	90 Ohm	L7	1
BC847C		Q1, Q2	2
4k7	1%	R23, R24, R25, R29	4
2k	1%	R46	1
1k	1%	R43, R47, R48, R50	4
10k	1%	R19, R20, R21, R22, R26, R27, R31, R32, R33, R34, R35, R37, R51, R52, R55, R56, R57, R61	18
1R	1%	R72	1

Continued on next page

Table C.0: *Bill of Materials (sorted by designator)*

Continued from previous page

Component	Specification	Designators	Count
0R	1%	R66, R70, R71, R81, R82, R86	6
51k	1%	R88	1
475k	1%	R90	1
604k	1%	R92	1
1.2M	1%	R91, R93	2
2.37M	1%	R94	1
63.4k	1%	R96	1
44.2k	1%	R98	1
100k	1%	R85, R100	2
200k	1%	R14, R54, R89, R95, R97, R99, R101, R102	8
33R	1%	R1, R2, R3, R4, R13, R15, R16, R17, R18, R38, R39, R40, R41, R60, R107, R108, R109, R110	18
12k	1%	R44, R45, R49, R111, R112, R113, R114, R115	8
200R	1%	R5, R6, R7, R8, R9, R10, R11, R12, R28, R30, R53, R78, R116	13
219-4MSTR	DIP switch 4 positions	SW1	1
PTS645-SK43	push button red	SW2	1
PTS645-SL43	push button black	SW3	1
CCGM1A1	GateMate FPGA	U1	1
SN74LVC08APWR		U2	1
NL27WZ04		U3	1
SN74LVC1G34DBVR		U4	1
MX25R6435FM2IH0	64 MBit	U5	1
MIC5504-3.3YMT-TZ		U6	1
FT2232HQ-Tray		U7	1
93LC56BT-I/OT		U8	1
MPM3833C		U9A, U9B, U9C, U9D, U9E	5
S27KS0641		U10	1
SN74CB3T3245PWR		U12A, U12B, U13, U14	4
SN74AUP2G00DCUR		U15	1
ECS-5032MV-100-BN-TR	10 MHz	X1	1
7M-12.000MAHV-T		X4	1

Acronyms

FPGA	field-programmable gate array	16
GPIO	general purpose input / output	5–7, 11, 16, 18, 24, 26, 29, 31, 33, 36, 37, 39, 44
JTAG	Joint Test Action Group	5, 11, 16, 27, 29, 44
LVDS	low-voltage differential signaling	5, 7, 31, 38, 39, 44
PCB	printed circuit board	5, 12, 16, 18, 21, 33, 44
Pmod	Pheripheral module interface (Digilent)	6, 7, 11, 24, 36, 44
SerDes	Serializer / Deserializer	5, 6, 11, 31, 38, 44
SPI	Serial Peripheral Interface	5, 11, 16, 27, 29, 44
USB	Universal Serial Bus	11, 16, 21, 22

GateMate™ FPGA
Evaluation Board Datasheet
Evaluation Board Version 3.1
DS1003
August 2022

Cologne Chip