High-Speed CMOS 512 x 36 x 2/1K x 36 x 2 Bi-directional FIFO

QS723611
QS723621

FEATURES/BENEFITS

- Fast cycle times: 20/25/30 ns (50/40/33 MHz)
- Functionally Upwards-Compatible with QS725420A
- Two 512 x 36-bit (QS723611) or 1K x 36-bit (QS723621) FIFO buffers
- Full 36-bit word width
- Selectable 36/18/9-bit word width on Port B
- Programmable 'Big-Endian to Little Endian' Conversion
- Synchronous request/acknowledge 'handshake' capability
- Asynchronous output enables
- Five status flags per port: Full, Almost-Full, Half-Full, Almost-Empty, and Empty
- All Flags are Independently Programmable for either Synchronous or Asynchronous Operation
- Almost-Full flag and Almost-Empty flag have Programmable Offsets
- Mailbox registers with synchronized flags
- Data-Bypass Function
- Data-Retransmit function
- Automatic byte parity checking
- Programmable Byte Parity Generation
- Programmable Byte-Oriented or Halfword-Oriented Parity Operations
- Space-saving 144-pin TQFP packages

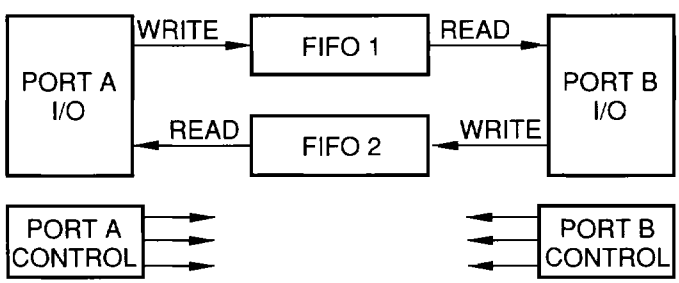
DESCRIPTION

The QS723611/21 contains two FIFO buffers, FIFO #1 and FIFO #2. These operate in parallel, but in opposite directions, for bi-directional data buffering. FIFO #1 and FIFO #2 each are organized as 512/1K words by 36 bits. The QS723611/21 is ideal either for wide unidirectional applications or for bi-directional data applications; component count and board area are reduced.

The QS723611/21 has two 36-bit ports, Port A and Port B. Each port has its own port-synchronous clock, but the two ports may operate asynchronously relative to each other. Data flow is initiated at a port by the rising edge of the appropriate clock; it is gated by the corresponding edge-sampled enable, request, and read/write control signals. At the maximum operating frequency, the clock duty cycle may vary from 40% to 60%. At lower frequencies, the clock waveform may be quite asymmetric, as long as the minimum pulse-width conditions for clock-HIGH and clock-LOW remain satisfied; the QS723611/21 is a fully static part.

Conceptually, the port clocks CKA and CKB are free-running, periodic "clock" waveforms, used to control other signals which are edge-sensitive. However, there actually is not any absolute requirement that these "clock" waveforms must be periodic. An "asynchronous" mode of operation is possible, in one or both directions, independently, if the appropriate en-

FIGURE 1. FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION *(Continued)*

able and request inputs are continuously asserted, and enough aperiodic "clock" pulses of suitable duration are generated by external logic to cause all necessary actions to occur.

A synchronous request/acknowledge handshake facility is provided at each port for FIFO data access. This request/acknowledge handshake resolves FIFO full and empty boundary conditions, when the two ports are operated asynchronously relative to each other.

FIFO status flags monitor the extent to which each FIFO buffer has been filled. Full, Almost-Full, Half-Full, Almost-Empty, and Empty flags are included for each FIFO. Each of these flags may be independently programmed for either synchronous or asynchronous operation. Also, the Almost-Full and Almost-Empty flags are programmable over the entire FIFO depth, but are automatically initialized to eight locations from the respective FIFO boundaries at reset. A data block of 512 (QS723611) or 1K (QS723621) or fewer words may be retransmitted any desired number of times.

Two mailbox registers provide a separate path for passing control words or status words between ports. Each mailbox has a new-mail-alert flag, which is synchronized to the reading port's clock. This mailbox function facilitates the synchronization of data transfers between asynchronous systems.

Data-bypass mode allows Port A to directly transfer data to or from Port B at reset. In this mode, the device acts as a registered transceiver under the control of Port A. For instance, a master processor on Port A can use the data bypass feature to send or receive initialization or configuration information directly, to or from a peripheral device on Port B, during system startup.

A word-width-select option is provided on Port B for 36-bit, 18-bit, or 9-bit data access. This feature allows word-width matching between Port A and Port B, with no additional logic needed. It also ensures maximum utilization of bus bandwidths. Subject to meeting timing requirements, the word-width selection may be changed at any time during the operation of the QS723611/21, without the need either for a reset operation or for passing dummy words through Port B immediately after the change; except that if the change is not made at a full-word boundary, at least one dummy word must be passed through Port B before any actual data words are transmitted.

A byte parity check flag at each port monitors data integrity. Control-register bit 00 (zero) selects the parity mode, odd or even. This bit is initialized for odd data parity at reset; but it may be reprogrammed for even parity, or back again to odd parity, as desired. The parity flags may be programmed to operate either in a latched mode or in a flowthrough mode. The parity checking may be performed over 36-bit full words, over 18-bit half-words, or over 9-bit single bytes.

Parity generation may be selected as well as parity checking, and may likewise be performed over full-words or half-words or single bytes. In any case, a parity bit of the proper mode is generated over the least-significant eight bits of a byte, and then is stored in the most significant bit position of the byte as it passes through the QS723611/21, overwriting whatever bit was present in that bit position previously.

FIGURE 2. FUNCTIONAL BLOCK DIAGRAM

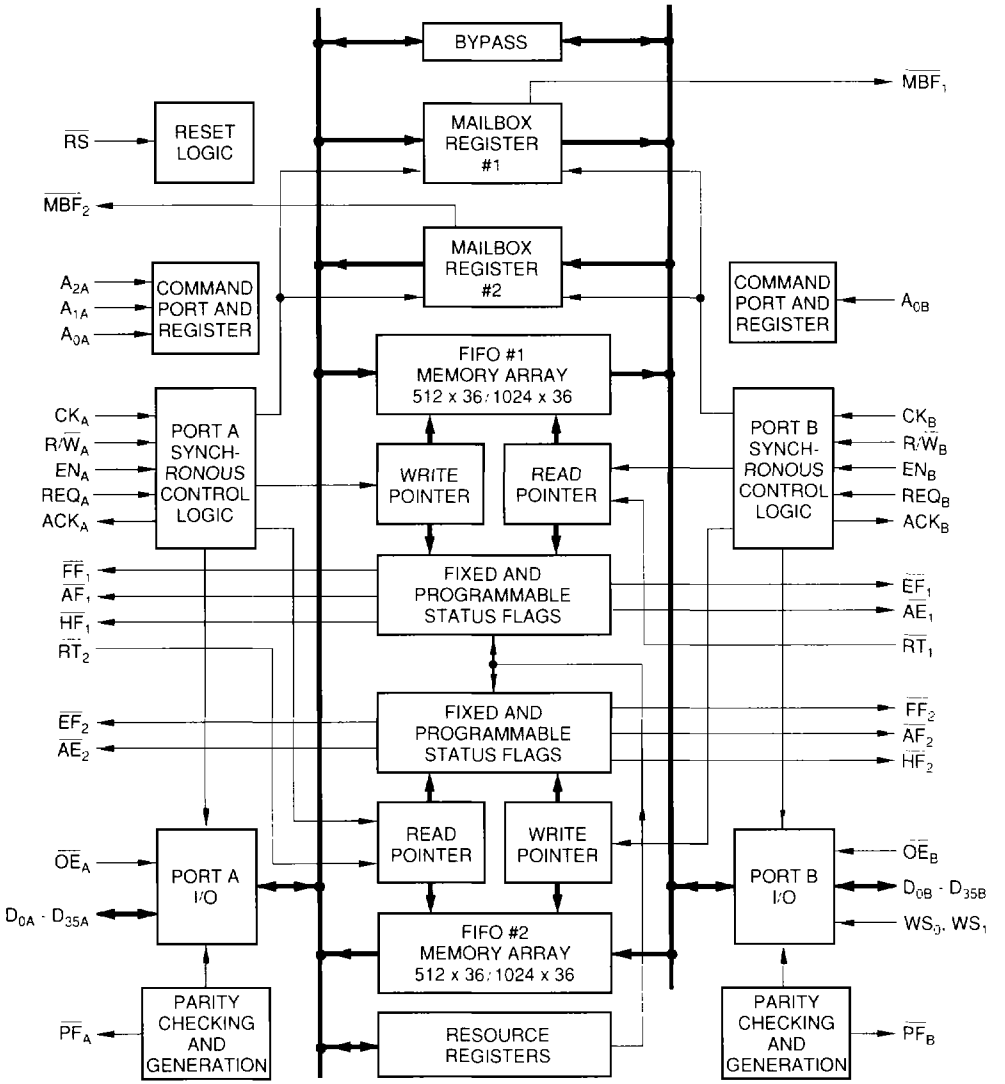
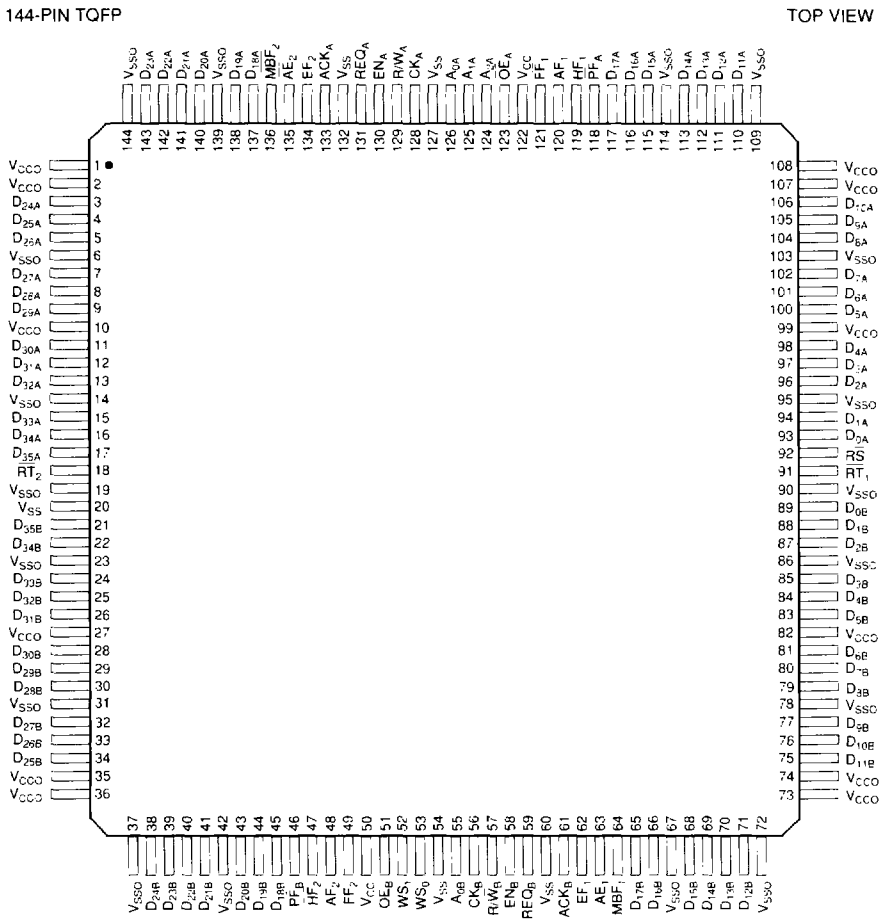


FIGURE 3. PINOUT

144-Pin TQFP
(Top view)



PIN DESCRIPTION

Signal Name	TQFP Pin No.
A0A	126
A1A	125
A2A	124
$\overline{OE}$A	123
$\overline{FF}$1	121
$\overline{AF}$1	120
$\overline{HF}$1	119
$\overline{PF}$A	118
D17A	117
D16A	116
D15A	115
D14A	113
D13A	112
D12A	111
D11A	110
D10A	106
D9A	105
D8A	104
D7A	102
D6A	101
D5A	100
D4A	98
D3A	97
D2A	96
D1A	94
D0A	93
$\overline{RS}$	92
$\overline{RT}$1	91
D0B	89
D1B	88
D2B	87
D3B	85
D4B	84
D5B	83
D6B	81
D7B	80
D8B	79
D9B	77
D10B	76
D11B	75
D12B	71
D13B	70
D14B	69
D15B	68
D16B	66
D17B	65
$\overline{MBF}$1	64
$\overline{AE}$1	63

Signal Name	TQFP Pin No.
$\overline{EF}$1	62
ACKB	61
REQB	59
ENB	58
R/$\overline{W}$B	57
CKB	56
A0B	55
WS0	53
WS1	52
$\overline{OE}$B	51
$\overline{FF}$2	49
$\overline{AF}$2	48
$\overline{HF}$2	47
$\overline{PF}$B	46
D18B	45
D19B	44
D20B	43
D21B	41
D22B	40
D23B	39
D24B	38
D25B	34
D26B	33
D27B	32
D28B	30
D29B	29
D30B	28
D31B	26
D32B	25
D33B	24
D34B	22
D35B	21
$\overline{RT}$2	18
D35A	17
D34A	16
D33A	15
D32A	13
D31A	12
D30A	11
D29A	9
D28A	8
D27A	7
D26A	5
D25A	4
D24A	3
D23A	143
D22A	142
D21A	141

Signal Name	TQFP Pin No.
D20A	140
D19A	138
D18A	137
$\overline{MBF}$2	136
$\overline{AE}$2	135
$\overline{EF}$2	134
ACKA	133
REQA	131
ENA	130
R/$\overline{W}$A	129
CKA	128
VCC	122
VSSO	114
VSSO	109
VCCO	108
VCCO	107
VSSO	103
VCCO	99
VSSO	95
VSSO	90
VSSO	86
VCCO	82
VSSO	78
VCCO	74
VCCO	73
VSSO	72
VSSO	67
VSS	60
VSS	54
VCC	50
VSSO	42
VSSO	37
VCCO	36
VCCO	35
VSSO	31
VCCO	27
VSSO	23
VSS	20
VSSO	19
VSSO	14
VCCO	10
VSSO	6
VCCO	2
VCCO	1
VSSO	144
VSSO	139
VSS	132
VSS	127

NOTES:
VCC = Supply internal logic. Connected to each other.
VCCO = Supply output drivers only. Connected to each other.
VSS = Supply internal logic. Connected to each other.
VSSO = Supply output drivers only. Connected to each other.

PIN DESCRIPTION

Name	Type[1]	Description
		GENERAL
Vcc, Vss	V	Power, Ground
$\overline{RS}$	I	Reset
		PORT A
CKA	I	Port A Free-Running Clock
R/$\overline{W}$A	I	Port A Edge-Sampled Read/Write Control
ENA	I	Port A Edge-Sampled Enable
A0A, A1A, A2A	I	Port A Edge-Sampled Address Pins
$\overline{OE}$A	I	Port A Level-Sensitive Output Enable
REQA	I	Port A Request/Enable
$\overline{RT}$2	I	FIFO #2 Retransmit
D35A-D0A	I/O/Z	Port A Bi-directional Data Bus
$\overline{FF}$1	O	FIFO #1 Full Flag (Write Boundary)
$\overline{AF}$1	O	FIFO #1 Programmable Almost-Full Flag (Write Boundary)
$\overline{HF}$1	O	FIFO #1 Half-Full Flag
$\overline{AE}$2	O	FIFO #2 Programmable Almost-Empty Flag (Read Boundary)
$\overline{EF}$2	O	FIFO #2 Empty Flag (Read Boundary)
$\overline{MBF}$2	O	New-Mail-Alert Flag for Mailbox #2
$\overline{PF}$A	O	Port A Parity Flag
ACKA	O	Port A Acknowledge
		PORT B
CKB	I	Port B Free-Running Clock
R/$\overline{W}$B	I	Port B Edge-Sampled Read/Write Control
ENB	I	Port B Edge-Sampled Enable
A0B	I	Port B Edge-Sampled Address Pin
$\overline{OE}$B	I	Port B Level-Sensitive Output Enable
WS0, WS1	I	Port B Word-Width Select
REQB	I	Port B Request/Enable
$\overline{RT}$1	I	FIFO #1 Retransmit
D35B-D0B	I/O/Z	Port B Bi-directional Data Bus
$\overline{FF}$2	O	FIFO #2 Full Flag (Write Boundary)
$\overline{AF}$2	O	FIFO #2 Programmable Almost-Full Flag (Write Boundary)
$\overline{HF}$2	O	FIFO #2 Half-Full Flag
$\overline{AE}$1	O	FIFO #1 Programmable Almost-Empty Flag (Read Boundary)
$\overline{EF}$1	O	FIFO #1 Empty Flag (Read Boundary)
$\overline{MBF}$1	O	New-Mail-Alert Flag for Mailbox #1
$\overline{PF}$B	O	Port B Parity Flag
ACKB	O	Port B Acknowledge

NOTES:
1. V = Power Voltage Level, I = Input, O = Output, Z = High Impedance.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground	−0.5V to +7.0V
DC Input Voltage V_{IN}[1]	−0.5V to Vcc + 0.5V
DC Output Current Max. Sink Current/Pin[2]	±40 mA
Maximum Power Dissapation	2W
Temperature Range with Power Applied	−55° to +125°C
T_{STG} Storage Temperature	−65° to +125°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional- or reliability-type failures.

Notes:
1. Negative undershoot of 1.5V in amplitude is permited for up to 10 ns, once per cycle.
2. Only one output may be shorted at a time, for a period not exceeding 30 Seconds.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C, Vcc = 5V ± 10%

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.2	Vcc + 0.5	V
V_{IL}	Input LOW Voltage[1]	Logic LOW for All Inputs	−0.5	0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = −8 mA	2.4	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 8 mA	—	0.4	V
I_{LO}	I/O Leakage	0V ≤ V_{OUT} ≤ Vcc, $\overline{OE}$ ≥V_{IH}	−10	+10	µA
I_{IL}	Input Leakage	Vcc = 5.5V, V_{IN} = 0V to Vcc	−10	+10	µA

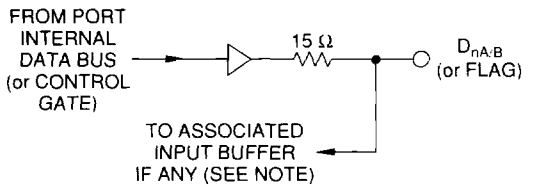
Note:
1. Negative undershoot of 1.5V in amplitude is permited for up to 10 ns, once per cycle.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
I_{CC}	Operating Current[1,2] fc = Max.	—	280	mA
I_{CC2}	Standby Current[1] All Inputs = V_{IHMIN} (Clocks Idle)	—	25	mA
I_{CC3}	Power Down Current[1] All Inputs at Vcc − 0.2V (Clocks Idle)	—	1	mA
I_{CC4}	Power Down Current[1] All Inputs at Vcc − 0.2V (Clocks at fc = Max.)	—	25	mA

Notes:
1. I_{CC}, I_{CC2}, I_{CC3}, and I_{CC4} are dependent upon actual output loading, and I_{CC} and I_{CC4} are also dependent on cycle rates. Specified values are with outputs open (for I_{CC}: C_{LSD} = 0 pF); and, for I_{CC} and I_{CC4}, operating at minimum cycle times.
2. I_{CC} using worst case conditions and data pattern.

FIGURE 4. STRUCTURE OF SERIES RESISTOR INPUT/OUTPUT INTERFACE

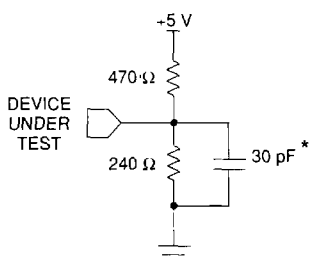


NOTE: Output-only pins have no associated input buffer.

AC TEST CONDITIONS

Input Pulse Levels	VSS to 3V
Input Rise/Fall Times (10% to 90%)	5 ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	30 pF

FIGURE 5. OUTPUT LOAD CIRCUIT



* INCLUDES JIG AND SCOPE CAPACITANCES

CAPACITANCE

T_A = 25°C, f = 1.0 MHz

Name	Description[1]	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	—	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	—	8	pF

Note:
1. *Capacitance is guaranteed but not tested.*

AC ELECTRICAL CHARACTERISTICS T_A = 0°C to +70°C, Vcc = 5V ± 10%

Symbol	Parameter[1]	Speed (ns) -20 Min	-20 Max	-25 Min	-25 Max	-30 Min	-30 Max	Units
fcc	Clock Cycle Frequency	—	50	—	40	—	33	MHz
tcc	Clock Cycle Time	20	—	25	—	30	—	ns
tch	Clock HIGH Time	8	—	10	—	12	—	ns
tcl	Clock LOW Time	8	—	10	—	12	—	ns
tds	Data Setup Time	7.5	—	9	—	10	—	ns
tdh	Data Hold Time	0.5	—	0.5	—	0.5	—	ns
tes	Enable Setup Time	5.5	—	7.5	—	8.5	—	ns
teh	Enable Hold Time	0.5	—	0.5	—	0.5	—	ns
trws	Read/Write Setup Time	5.5	—	7.5	—	8.5	—	ns
trwh	Read/Write Hold Time	0.5	—	0.5	—	0.5	—	ns
trqs	Request Setup Time	5.5	—	7.5	—	8.5	—	ns
trqh	Request Hold Time	0.5	—	0.5	—	0.5	—	ns
tas	Address Setup Time[2]	7.5	—	9	—	10	—	ns
tah	Address Hold Time[2]	0.5	—	0.5	—	0.5	—	ns
twss	Width Select Setup Time	5.5	—	7.5	—	8.5	—	ns
twsh	Width Select Hold Time[3]	0.5	—	0.5	—	0.5	—	ns
ta	Data Output Access Time	—	13.8	—	16	—	20	ns
tack	Acknowledge Access Time	—	9.5	—	13	—	16	ns
toh	Output Hold Time	4	—	4	—	4	—	ns
tzx	Output Enable Time $\overline{OE}$ LOW to D35-D0 LOW-Z[3]	1.5	—	2	—	3	—	ns
txz	Output Disable Time $\overline{OE}$ HIGH to D35-D0 HIGH-Z[3]	—	9	—	12	—	15	ns
tef	Clock to $\overline{EF}$ Flag Valid (Empty Flag)	—	14.5	—	19	—	22	ns
tff	Clock to $\overline{FF}$ Flag Valid (Full Flag)	—	14.5	—	19	—	22	ns
thf	Clock to $\overline{HF}$ Flag Valid (Half-Full Flag)	—	14.5	—	19	—	22	ns
tae	Clock to $\overline{AE}$ Flag Valid (Almost-Empty Flag)	—	15	—	19	—	22	ns
taf	Clock to $\overline{AF}$ Flag Valid (Almost-Full Flag)	—	15	—	19	—	22	ns
tmbf	Clock to $\overline{MBF}$ Flag Valid (Mailbox Flag)	—	10	—	13	—	18	ns
tpf	Data to Parity Flag Valid[4]	—	14	—	17	—	20	ns
trs	Reset/Retransmit Pulse Width[5]	20	—	25	—	30	—	ns
trss	Reset/Retransmit Setup Time[6]	16	—	20	—	25	—	ns
trsh	Reset/Retransmit Hold Time[6]	8	—	10	—	15	—	ns
trf	Reset LOW to Flag Valid	—	21	—	25	—	30	ns
tfrl	First Read Latency[7]	20	—	25	—	30	—	ns
tfwl	First Write Latency[8]	20	—	25	—	30	—	ns
tbs	Bypass Data Setup	8.5	—	10	—	13	—	ns
tbh	Bypass Data Hold	2	—	3	—	4	—	ns
tba	Bypass Data Access	—	16	—	18	—	23	ns
tskew1	Skew Time Read-to-Write Clock[3]	14.5	—	19	—	22	—	ns
tskew2	Skew Time Write-to-Read Clock[3]	14.5	—	19	—	22	—	ns

Notes:

1. Timing measurements performed at AC TEST CONDITION levels.
2. tas, tah address setup times and hold times need only be satisfied at clock edges which occur while the corresponding enables are being asserted.
3. Values are guaranteed by design, not currently production tested.
4. Measured with Parity Flag operating in flowthrough mode.
5. When CKa or CKb is enabled: trs = trss + tch + trsh.
6. trss and/or trsh need not be met unless a rising edge of CKa occurs while ENa is being asserted, or else a rising edge of CKb occurs while ENb is being asserted.
7. tfrl is the minimum first-write-to-first-read delay, following an empty condition, which is required to assure valid read data.
8. tfwl is the minimum first-read-to-first-write delay, following a full condition, which is required to assure successful writing of data.

OPERATIONAL DESCRIPTION

Reset

The device is reset whenever the asynchronous reset ($\overline{RS}$) input is taken LOW, and at least one rising edge and one falling edge of both CLKA and CLKB occur while $\overline{RS}$ is LOW. A reset operation is required after power-up, before the first write operation may occur. The QS723611/21 is fully ready for operation after being reset. No device programming is required if the default states described below are acceptable.

A reset operation initializes the read-address and write-address pointers for FIFO #1 and FIFO #2 to those FIFOs' first physical memory locations. If the respective outputs are enabled, the initial contents of these first locations appear at the outputs. FIFO and mailbox status flags are updated to indicate an empty condition. In addition, the programmable-status-flag offset values are initialized to eight. Thus, the $\overline{AE1}$/$\overline{AE2}$ flags get asserted within eight locations of an empty condition, and the $\overline{AF1}$/$\overline{AF2}$ flags likewise get asserted within eight locations of a full condition, for FIFO #1/FIFO #2, respectively.

Bypass Operation

During reset (whenever $\overline{RS}$ is LOW) the device acts as a registered transceiver, bypassing the internal FIFO memories. Port A acts as the master port. A write or read operation on Port A during reset transfers data directly to or from Port B. Port B is considered to be the slave, and cannot perform write or read operations independently on its own during reset.

The direction of the bypass data transmission is determined by the R/$\overline{W}$A control input, which does not get overridden by the $\overline{RS}$ input. Here, a "write" operation means passing data from Port A to Port B, and a "read" operation means passing data from Port B to Port A.

The bypass capability may be used to pass initialization or configuration data directly between a master processor and a peripheral device during reset.

Address Modes

Address pins select the device resource to be accessed by each port. Port A has three resource-register-select inputs, A0A, A1A and A2A, which select between FIFO access, mailbox-register access, control-register access, and programmable flag-offset-value register access. Port B has a single address input, A0B, to select between FIFO access or mailbox-register access.

TABLE 1. RESOURCE-REGISTER ADDRESSES

A2A	A1A	A0A	Resource
PORT A			
H	H	H	FIFO
H	H	L	Mailbox
H	L	H	$\overline{AF2}$, $\overline{AE2}$, $\overline{AF1}$, $\overline{AE1}$ Flag Offset Registers (36-bit Mode)
H	L	L	Control Registers Flag-Synchronization and Parity Operating Mode
L	H	H	$\overline{AE1}$ Flag Offset Registers
L	H	L	$\overline{AF1}$ Flag Offset Registers
L	L	H	$\overline{AE2}$ Flag Offset Registers
L	L	L	AF2 Flag Offset Registers
A0B			Resource
PORT B			
H			FIFO
L			Mailbox

The status of the resource-register-select inputs is sampled at the rising edge of an enabled clock (CKA or CKB). Resource-register select-input address definitions are summarized in Table 1.

Control Register

The eighteen Control-Register bits govern the synchronization mode of the fullness-status flags at each port, the choice of odd or even parity at both ports, the enabling of parity generation for data flow at each port, the optional latching behavior of the parity-error flags at each port, and the selection of a full-word or half-word or single-byte field for parity checking. A reset operation initializes the QS723611/21 Control Register for QS725420 compatible operation, but it may be reprogrammed at will at any time during QS723611/21 operation.

FIFO Write

Port A writes to FIFO #1, and Port B writes to FIFO #2. A write operation is initiated on the rising edge of a clock (CKA or CKB) whenever the appropriate enable (ENA or ENB) is held HIGH; the appropriate request (REQA or REQB) is held HIGH; the appropriate read/write control (R/$\overline{W}$A a R/$\overline{W}$B) is held LOW; the FIFO address is selected for the address inputs (A2A-A0A or A0B); and the prescribed setup times and hold times are observed for all of these signals. Setup times and hold times must also be observed on the data-bus pins (D0A-D35A or D0B-D35B).

Normally, the appropriate output enable signal ($\overline{OE}_A$ or $\overline{OE}_B$) is HIGH, to disable the outputs at that port, so that the data word present on the bus from external sources gets stored. However, a "loopback" mode of operation also is possible, in which the data word supplied by the outputs of one internal FIFO is "turned around" at the port and read back into the other FIFO. In this mode, the outputs at the port are not disabled. To remain within specification for all timing parameters, the clock cycle frequency must be reduced slightly below the value which otherwise would be permissible for that speed grade of QS723611/21.

When a FIFO full condition is reached, write operations are locked out. Following the first read operation from a full FIFO, another memory location is freed up, and the corresponding full flag is de-asserted ($\overline{FF}$ = HIGH). The first write operation should begin no earlier than a first write latency (t_{FWL}) after the first read operation from a full FIFO, to ensure that correct read data are retrieved.

FIFO Read

Port A reads from FIFO #2 and Port B reads from FIFO #1. A read operation is initiated on the rising edge of a clock (CK_A or CK_B) whenever: the appropriate enable (EN_A or EN_B) is held HIGH; the appropriate request (REQ_A or REQ_B) is held HIGH; the appropriate read/write control ($R/\overline{W}_A$ or $R/\overline{W}_B$) is held HIGH; the FIFO address is selected for the address inputs ($A2_A$-$A0_A$ or A0); and the prescribed setup times and hold times are observed for all of these signals. Read data becomes valid on the data-bus pins ($D35_A$-$D0_A$ or $D35_B$-$D0_B$) by a time t_A after the rising clock (CK_A or CK_B) edge, provided that the data outputs are enabled.

$\overline{OE}_A$ and $\overline{OE}_B$ are assertive LOW, asynchronous, output enable control input signals. Their effect is only to enable or disable the output drivers of the respective port. Disabling the outputs does not disable a read operation; data transmitted to the corresponding output register will remain available later, when the outputs again are enabled, unless it subsequently is overwritten.

When an empty condition is reached, read operations are locked out until a valid write operation(s) has loaded additional data into the FIFO. Following the first write to an empty FIFO, the corresponding empty flag ($\overline{EF}$) will be de-asserted (HIGH). The first read operation should begin no earlier than a first read latency (t_{FRL}) after the first write to an empty FIFO, to ensure that correct read data is retrieved.

Dedicated FIFO Status Flags

Six dedicated FIFO status flags are included for full ($\overline{FF}$ and $\overline{FF2}$), half-full ($\overline{HF}$ and $\overline{HF2}$), and empty ($\overline{EF}$ and $\overline{EF2}$). $\overline{FF}$, $\overline{HF}$, and $\overline{EF}$ indicate the status of FIFO #1; and $\overline{FF2}$, $\overline{HF2}$, and $\overline{EF2}$ indicate the status of FIFO #2.

A Full flag is asserted following the rising clock edge for a write operation that fills the FIFO. A Full flag is de-asserted following the falling clock edge for a read operation to a full FIFO. A Half-Full flag is updated following the rising clock edge of a read or write operation to a FIFO. An Empty flag is asserted following the rising clock edge for a read operation that empties the FIFO. An Empty flag is de-asserted following the falling clock edge for a write operation to an empty FIFO.

Programmable Status Flags

Four programmable FIFO status flags are provided: two for almost-full ($\overline{AF}$ and $\overline{AF2}$), and two for almost-empty ($\overline{AE}1$ and $\overline{AE}2$). Thus, each port has two programmable flags to monitor the status of the two internal FIFO buffer memories. The offset values for these flags are initialized to eight locations from the respective FIFO boundaries during reset but can be reprogrammed over the entire FIFO depth.

An Almost-Full flag is asserted following the rising clock edge for a write operation which has partially filled the FIFO up to the 'almost-full' offset point. An Almost-Full flag is de-asserted following the first subsequent falling clock edge after a read operation which has partially emptied the FIFO down past the 'almost-full' offset point. An Almost-Empty Flag is asserted following the first subsequent rising clock edge after a read operation which has partially emptied the FIFO down to the 'almost empty' offset point. An Almost-Empty Flag is deasserted following the first subsequent falling clock edge after a write operation which has partially filled the FIFO up past the 'almost-empty' offset point.

Flag offsets may be written or read through the Port A data bus. All four programmable FIFO status flag offsets can be set simultaneously through a single 36-bit status word, or each programmable flag offset can be set individually, through one of four 9-bit (QS723611) or 10-bit (QS723621) status words. Table 3A and 3B illustrates the data format for flag-programming words. Note that when all four offsets are set simultaneously in a QS723621, the settings are limited to magnitudes expressible in nine bits; for larger offset values, the individual setting option must be used (See Figure 3B).

Also, Tables 4A and 4B defines the meaning of each of the five flags, both the dedicated flags and the flag-programming flags, for the QS723611 and QS723621 respectively.

NOTE: Control inputs which may affect the computation of flag values at a port generally should not change while the clock for that port is HIGH, since some updating of flag values takes place on the falling edge of the clock.

Mailbox Operation

Two mailbox registers are provided for passing system hardware or software control/status words between ports. Each port can read its own mailbox and write to the other port's mailbox. Mailbox access is performed on the rising edge of the controlling FIFO's clock, with the mailbox address selected and the enable (ENA or ENB) HIGH. That is, writing to mailbox register #1, or reading from mailbox register #2, is synchronized to CK_A; and writing to mailbox register #2, or reading from mailbox register #1, is synchronized to CK_B.

The $R/\overline{W}_{A/B}$ and $\overline{OE}_{A/B}$ pins control the direction and availability of mailbox-register accesses. Each mailbox register has its own New-Mail-Alert Flag ($\overline{MBF1}$ and $\overline{MBF2}$), which is synchronized to the reading port's clock. These new-mail-alert flags are status indicators only and cannot inhibit mailbox-register read or write operations.

Request Acknowledge Handshake

A synchronous, request-acknowledge handshake feature is provided for each port, to perform boundary synchronization between asynchronous-operated ports. The use of this feature is optional. When it is used, the request input ($REQ_{A/B}$) is sampled at a rising clock edge. With $REQ_{A/B}$ HIGH, $R/\overline{W}_{A/B}$ determines whether a FIFO read operation or a FIFO write operation is being requested. The acknowledge output ($ACK_{A/B}$) is updated during the following clock cycle(s). $ACK_{A/B}$ meets the setup and hold time requirements of the enable input (EN_A or EN_B). Therefore, $ACK_{A/B}$ may be tied back to the enable input to directly gate FIFO accesses, at a slight decrease in maximum operating frequency.

The assertion of $ACK_{A/B}$ signifies that $REQ_{A/B}$ was asserted. However, $ACK_{A/B}$ does not depend logically on $EN_{A/B}$; and thus the assertion of $ACK_{A/B}$ does not prove that a FIFO write access or a FIFO read access actually took place. While $REQ_{A/B}$ and $EN_{A/B}$ are being held HIGH, $ACK_{A/B}$ may be considered as a synchronous, predictive boundary flag. That is, $ACK_{A/B}$ acts as a synchronized predictor of the Almost-Full flag $\overline{AF}$ for write operations, or as a synchronized predictor of the Almost-Empty flag $\overline{AE}$ for read operations.

Outside the "almost-full" region and the "almost-empty" region, $ACK_{A/B}$ remains continuously HIGH whenever $REQ_{A/B}$ is held continuously HIGH. Within the "almost-full" region or the "almost-empty" region, $ACK_{A/B}$ occurs only on every third cycle, to prevent an overrun of the FIFO's actual full or empty boundaries, and to ensure that the t_{FWL} (first-write latency) and t_{FRL} (first-read latency) specifications are satisfied before $ACK_{A/B}$ is received.

The "almost-full region" is defined as "that region, where the Almost-Full flag is being asserted"; and the "almost-empty region" as "that region, where the Almost-Empty flag is being asserted." Thus, the extent of these "almost" regions depends on how the system has programmed the offset values for the Almost-Full flags and the Almost-Empty flags. If the system has not programmed them, then these offset values remain at their default values, eight in each case.

If a write attempt is unsuccessful because the corresponding FIFO is full, or if a read attempt is unsuccessful because the corresponding FIFO is empty, $ACK_{A/B}$ is not asserted in response to $REQ_{A/B}$.

If the REQ/ACK handshake is not used, then the $REQ_{A/B}$ input may be used as a second enable input, at a possible minor loss in maximum operating speed. In this case, the $ACK_{A/B}$ output may be ignored.

NOTE: Whether or not the REQ/ACK handshake is being used, the $REQ_{A/B}$ input for a port must be asserted for that port to function at all-for FIFO, mailbox, or data-bypass operation.

Data Retransmit

A retransmit operation resets the read-address pointer of the corresponding FIFO (#1 or #2) back to the first FIFO physical memory location, so that data may be reread. The write pointer is not affected. The status flags are updated, and a block of up to 512/1K data words, which previously had been written into and read from a FIFO, can be retrieved. The block to be retransmitted is bounded by the first FIFO memory location and the FIFO memory location addressed by the write pointer. FIFO #1 retransmit is initiated by strobing the $\overline{RT1}$ pin LOW. FIFO #2 retransmit is initiated by strobing the $\overline{RT2}$ pin LOW. Read and write operations to a FIFO should be stopped while the corresponding retransmit signal is being asserted.

Parity Checking

The Parity check flags, $\overline{PF}_A$ and $\overline{PF}_B$, are asserted (LOW) whenever there is a parity error in the data word present on the Port A data bus or the Port B data bus, respectively. The inputs to the parity-evaluation logic come directly (via isolation transistors) from the data-bus bonding pads, in each case. Thus, $\overline{PF}_A$ and $\overline{PF}_B$ provide parity-error indications for whatever 36-bit words are present at Port A and Port B, respectively, regardless of whether these words originated within the QS723611/21 or in the external system.

The four bytes of a 36-bit data word are grouped as D0-D8, D9-D17, D18-D26, and D27-D35. The parity of each 9-bit byte is individually checked, and the four single-bit parity indications are logically inclusive-ORed and inverted to produce the parity-flag output.

If the Parity Policy bit (Control-Register bit 09) is HIGH, then parity at Port B will be computed over the field defined by the Word-Width Selection control inputs WS0 and WS1, and then may be for full-words, for half-words, or for single bytes. Otherwise, parity will be computed over full-words regardless of the setting of WS0 andWS1.

Parity checking is initialized for odd parity at reset, but can be reprogrammed for even parity or for odd parity during operation. Control-register bit 0 (zero) selects the parity mode, odd or even (see Tables 3, 5, and 6 and Figure 6).

All nine bits of each byte are treated alike by the parity logic. The byte parity over the nine bits is compared with the parity mode bit in the control register, to generate a byte-parity-error indication. Then, the four byte-parity-error signals are NORed together, to compute the assertive-LOW parity-flag value. This value may pass through to the output pin on a flowthrough basis, or it may be latched, according to the setting of the Control-Register latching bit for that port (bit 02 or bit 11).

Parity Generation

Unlike parity checking, parity generation at a port operates only when it is explicitly invoked by setting the corresponding Control-Register bit for that port (bit 01 or bit 10) HIGH. The presumed division of words into bytes still remains the same as for parity checking. However, it is no longer true that all nine bits of each byte are treated alike; now, the most-significant bit of each byte is explicitly designated as the parity bit for the byte. The parity-generation process records a new value into that bit position for each byte passing through the port.

If the Parity Policy bit (Control Register 09) is HIGH, parity at Port B will be generated for full-words, for half-words, or for single bytes according to the setting of the Word-Width Selection control inputs WS0 and WS1. Otherwise, parity will be generated for full-words regardless of the setting of WS0 and WS1.

The parity bits generated may be even or odd, according to the setting of Control Register bit 00, which is the same bit that governs their interpretation during parity checking.

Word-Width Selection and Byte-Order Reversal on Port B

The word width of data access on Port B is selected by the WS0 and WS1 control inputs. WS0 and WS1 both are tied HIGH for 36-bit access; they both are tied LOW for single-byte access. For double-byte access, WS1 is tied LOW; WS0 is tied HIGH for straight-through transmission of 36-bit words, or tied LOW for on-the-fly byte-order reversal of the four bytes in the word ('big-endian to little endian conversion'). (See Table 2).

In the single-byte-access or double-byte access modes, FIFO write operations on Port B essentially pack the data to form 36-bit words, as viewed from Port A. Similarly, single-byte or double-byte FIFO read operations on Port B essentially unpack 36-bit words through a series of shift operations. FIFO status flags are updated following the last access which forms a complete 36-bit transfer.

Since the values for each status flag are computed by logic directly associated with one of the two FIFO-memory arrays, and not by logic associated with Port B, the flag values reflect the array fullness situation in terms of complete 36-bit words, and not in terms of bytes or double bytes.

TABLE 2. PORT B WORD-WIDTH SELECTION

WS1	WS0	Port B Data Width
H	H	36-Bit
H	L	36-Bit with Byte Order Reversal
L	H	18-Bit
L	L	9-Bit

However, there is no such restriction for switching from writing to reading, or from reading to writing, at Port B. As long as t_{RWS}, t_{DS}, and t_A are satisfied, R/$\overline{W}_B$ may change state after any single-byte or double-byte access, and not only after a full 36-bit-word access.

Also, WS0 and WS1 may be changed between full-words during FIFO operation, without the need for any reset operation, or for passing any dummy words on through in advance of real data. If such a change is made other than at a full-word boundary, however, at least one dummy word should be used.

Also, the word-width-matching feature continues to operate properly in "loopback" mode.

Note that the programmable word-width-matching feature is only supported for FIFO accesses. Mailbox and data bypass operations do not support word-width matching between Port A and Port B. Tables 2 and Figures 7 and 8 summarize word-width selection for Port B.

TABLE 3A. QS723611 RESOURCE-REGISTER PROGRAMMING

Resource-Register Address A_{2A}	A_{1A}	A_{0A}	Resource-Register Contents
			NORMAL FIFO OPERATION
			D35A ... **D0A**
H	H	H	X... ...X
			MAILBOX
			D35A ... **D0A**
H	H	L	X... ...X
			$\overline{AF}$2, $\overline{AE}$2, $\overline{AF}$1, $\overline{AE}$1 FLAG REGISTER (36-BIT MODE)
			D35A-D27A | **D26A-D18A** | **D17A-D9A** | **D8A-D0A**
H	L	H	$\overline{AF}$2 Offset[1] | $\overline{AE}$2 Offset[1] | $\overline{AF}$1 Offset[1] | $\overline{AE}$1 Offset[1]
			CONTROL REGISTER: FLAG SYNCHRONIZATION, PARITY CONFIGURATION
			D35A ... **D18A** **D17A** ... **D9A** **D8A** ... **D1A** **D0A**
H	L	L	X... ...X | Port B Control[3] | Port A Control[3] | PM[2]
			9-BIT $\overline{AE}$1 FLAG OFFSET REGISTER
			D35A ... **D9A** **D8A-D0A**
L	H	H	X... ...X | $\overline{AE}$1 Offset[1]
			9-BIT $\overline{AF}$1 FLAG OFFSET REGISTER
			D35A ... **D9A** **D8A-D0A**
L	H	L	X... ...X | $\overline{AF}$1 Offset[1]
			9-BIT $\overline{AE}$2 FLAG OFFSET REGISTER
			D35A ... **D9A** **D8A-D0A**
L	L	H	X... ...X | $\overline{AE}$2 Offset[1]
			9-BIT $\overline{AF}$2 FLAG OFFSET REGISTER
			D35A ... **D9A** **D8A-D0A**
L	L	L	X... ...X | $\overline{AF}$2 Offset[1]

Notes:
1. All four programmable-flag offset values are initialized to eight (8) during a reset operation.
2. Odd parity = HIGH; even parity = LOW. The parity mode is initialized to odd during a reset operation.
3. See Tables 5 and 6 and Figure 6 for the detailed format of the Control Register word.

TABLE 3B. QS723621 RESOURCE-REGISTER PROGRAMMING

Resource-Register Address A_{2A}	A_{1A}	A_{0A}	Resource-Register Contents						
			NORMAL FIFO OPERATION						
			D35A						**D0A**
H	H	H	X...						...X
			MAILBOX						
			D35A						**D0A**
H	H	L	X...						...X
			$\overline{AF}$2, $\overline{AE}$2, $\overline{AF}$1, $\overline{AE}$1 FLAG REGISTER (36-BIT MODE)[4]						
			D35A-D27A	**D26A-D18A**	**D17A-D9A**	**D8A-D0A**			
H	L	H	$\overline{AF}$2 Offset[1]	$\overline{AE}$2 Offset[1]	$\overline{AF}$1 Offset[1]	$\overline{AE}$1 Offset[1]			
			CONTROL REGISTER: FLAG SYNCHRONIZATION, PARITY CONFIGURATION						
			D35A	**D18A**	**D17A**	**D9A**	**D8A**	**D1A**	**D0A**
H	L	L	X...	...X	Port B Control[3]		Port A Control[3]		PM[2]
			10-BIT $\overline{AE}$1 FLAG OFFSET REGISTER						
			D35A			**D10A**	**D9A-D0A**		
L	H	H	X...			...X	$\overline{AE}$1 Offset[1]		
			10-BIT $\overline{AF}$1 FLAG OFFSET REGISTER						
			D35A			**D10A**	**D9A-D0A**		
L	H	L	X...			...X	$\overline{AF}$1 Offset[1]		
			10-BIT $\overline{AE}$2 FLAG OFFSET REGISTER						
			D35A			**D10A**	**D9A-D0A**		
L	L	H	X...			...X	$\overline{AE}$2 Offset[1]		
			10-BIT $\overline{AF}$2 FLAG OFFSET REGISTER						
			D35A			**D10A**	**D9A-D0A**		
L	L	L	X...			...X	$\overline{AF}$2 Offset[1]		

Notes:
1. All four programmable-flag offset values are initialized to eight (8) during a reset operation.
2. Parity Mode: Odd parity = HIGH; even parity = LOW. The parity mode is initialized to odd during a reset operation.
3. See Tables 5 and 6 and Figure 6 for the detailed format of the Control Register word.
4. For 36-bit Flag Register Control word. with only 9 bits to program per flag offset:
   Offset is limited to a value of 511. If a greater value is desired. individual flag offset register programming is required.

TABLE 4A. QS723611 FLAG DEFINITION TABLE

	Valid Full-Word Read Cycles Remaining				Valid Full-Word Write Cycles Remaining			
	Flag = LOW		Flag = HIGH		Flag = LOW		Flag = HIGH	
Flag	Min	Max	Min	Max	Min	Max	Min	Max
$\overline{FF}$	512	512	0	511	0	0	1	512
$\overline{AF}$	512 – p	512	0	511 – p	0	p	p + 1	512
$\overline{HF}$	257	512	0	256	0	255	256	512
$\overline{AE}$	0	q	q + 1	512	512 – q	512	0	511 – q
$\overline{EF}$	0	0	1	12	512	512	0	511

Note:

1. q = Programmable almost-empty offset value (default value: q = 8).
   p = Programmable almost-full offset value (default value: p = 8).

TABLE 4B. QS723621 FLAG DEFINITION TABLE

	Valid Full-Word Read Cycles Remaining				Valid Full-Word Write Cycles Remaining			
	Flag = LOW		Flag = HIGH		Flag = LOW		Flag = HIGH	
Flag	Min	Max	Min	Max	Min	Max	Min	Max
$\overline{FF}$	1024	1024	0	1023	0	0	1	1024
$\overline{AF}$	1024 – p	1024	0	1023 – p	0	p	p + 1	1024
$\overline{HF}$	513	1024	0	512	0	511	512	1024
$\overline{AE}$	0	q	q + 1	1024	1024 – q	1024	0	1023 – q
$\overline{EF}$	0	0	1	1024	1024	1024	0	1023

Note:

1. q = Programmable almost-empty offset value (default value: q = 8).
   p = Programmable almost-full offset value (default value: p = 8).

TABLE 5. CONTROL REGISTER FORMAT

PORT	COMMAND REGISTER BITS	CODE	VALUE AFTER RESET	FLAGS AFFECTED, IF ANY	DESCRIPTION	NOTES
A, B	00	L	H	$\overline{PF_A}$, $\overline{PF_B}$	EVEN parity in effect.	A correct 9-bit byte has an even number of ones.
		H			ODD parity in effect	A correct 9-bit byte has an odd number of ones.
A	01	L	L	–	Disable Port A pairty generation.	No overwriting of parity bits.
		H			Enable Port A pairty generation	Parity bit over eight least-significant bits of each byte is overwritten into the most-significant bit of that byte
	02	L	L	$\overline{PF_A}$	Port A parity-error flag operates 'flow-through.'	PFA# is subject to transient glitches while data bus is changing
		H			Port A parity-error flag is latched by CKA	PFA# remains steady until its value should change.
	03	L	L	$\overline{EF2}$	Set by ^ CKA, reset by ^ CKB.	Asynchrouous flag clocking
		H			Set and reset by ^ CKA.	Synchronous flag clocking.
	04	L	L	$\overline{AE2}$	Set by ^ CKA, reset by ^ CKB	Asynchronous flag clocking.
		H			Set and reset by ^ CKA.	Synchronous flag clocking.
	06, 05	LL	LL	$\overline{HF1}$	Set by ^ CKA, reset by ^ CKB	Asynchronous flag clocking
		LH			Set and reset by ^ CKB.	Synchronous flag clocking by Port B clock.
		HL, HH			Set and reset by ^ CKA	Synchronous flag clocking by Port A clock
	07	L	L	$\overline{AF1}$	Set by ^ CKA, reset by ^ CKB	Asynchronous flag clocking.
		H			Set and reset by ^ CKA	Synchronous flag clocking
	08	L	L	$\overline{FF1}$	Set by ^ CKA, reset by ^ CKB.	Asynchronous flag clocking.
		H			Set and reset by ^ CKA	Synchronous flag clocking.
B	09	L	L	$\overline{PF_B}$	Parity check computed over all four bytes of each word	Full-word parity-error indication regardless of WS1-WS0 setting.
		H			Parity check computed over half-word or single-byte according to WS1-WS0 setting.	Full-word, half-word, or single-byte parity-error indication according to WS1-WS0 setting.
	10	L	L	–	Disable Port B parity *generation*	No overwriting of parity bits.
		H			Enable Port B parity generation	Parity bit over eight least-significant bits of each byte is overwritten into the most-significant bit of that byte.
	11	L	L	$\overline{PF_B}$	Port B parity-error flag operates 'flowthrough'	$\overline{PF_B}$ is subject to transiet glitches while data bus is changing
		H			Port B parity-error flag is latched by CKB.	$\overline{PF_B}$ remains steady until its value should change.
	12	L	L	$\overline{EF1}$	Set by ^ CKB reset by ^ CKA	Asynchronous flag clocking
		H			Set and reset by ^ CKB.	Synchronous flag clocking
	13	L	L	$\overline{AE1}$	Set by ^ CKB, reset by ^ CKA	Asynchronous flag clocking.
		H			Set and reset by ^ CKB.	Synchronous flag clocking
	15, 14	LL	LL	$\overline{HF2}$	Set by ^ CKB, reset by ^ CKA.	Asynchronous flag clocking.
		LH			Set and reset by ^ CKA.	Synchronous flag clocking by Port A clock
		HL, HH			Set and reset by ^ CKB	Synchronous flag clocking by Port B clock

TABLE 5. CONTROL REGISTER FORMAT (Continued)

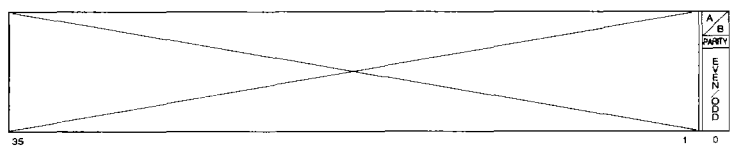
PORT	COMMAND REGISTER BITS	CODE	VALUE AFTER RESET	FLAGS AFFECTED, IF ANY	DESCRIPTION	NOTES
B	16	L	L	$\overline{AF}2$	Set by ^ CKB, reset by ^ CKA.	Asynchrouous flag clocking.
		H			Set and reset by ^ CKB.	Synchrouous flag clocking.
	17	L	L	$\overline{FF}2$	Set by ^ CKB, reset by ^ CKA.	Asynchrouous flag clocking.
		H			Set and reset by ^ CKB.	Synchrouous flag clocking.

TABLE 6. CONTROLLABLE FUNCTIONS

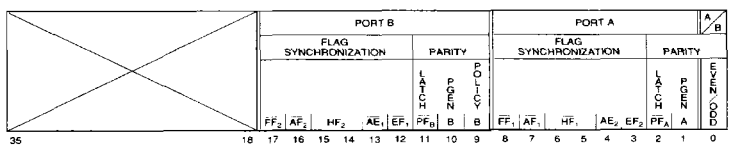
TYPE	DESCRIPTION	CONTROL REGISTER BIT	
		PORT A	PORT B
Parity	Even/Odd	0[1]	0[1]
	Policy for 9/18-Bit Word Width Selection	-	9
	Generation: Enable/Disable	1	10
	Flag Behavior: Latched/Flowthrough	2	11
Flag Synchronization	$\overline{EF}$ Synchronous/Asynchronous	3	12
	$\overline{AE}$ Synchronous/Asynchronous	4	13
	$\overline{HF}$ Synchronous-With-Write/Synchronous-With-Read	5-6	14-15
	$\overline{AF}$ Synchronous/Asynchronous	7	16
	$\overline{FF}$ Synchronous/Asynchronous	8	17

Notes:
1. The QS723611/21 also have this Control-Register function. The same Control-Register bit, bit 00, controls both Port A and Port B functionality.

FIGURE 6. QS723611/21 CONTROL REGISTER FORMATS



QS725420 CONTROL REGISTER (WRITE-ONLY)
(FOR COMPARISON PURPOSES)



QS723611/21 CONTROL REGISTER (READ/WRITE)

PORT B WORD-WIDTH SELECTION

FIGURE 7A. 36-18 FUNNELING THROUGH FIFO #1

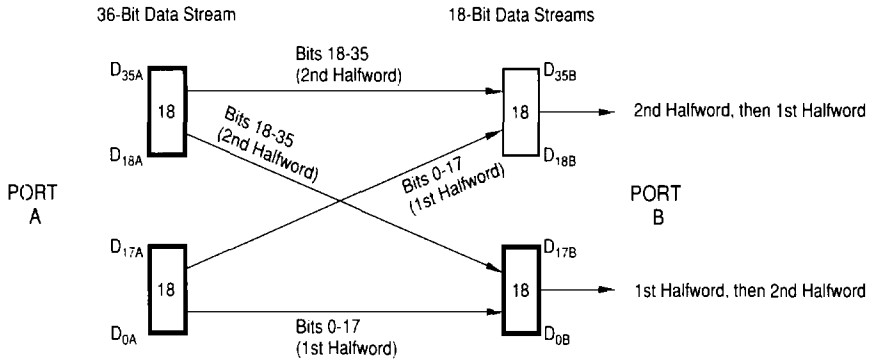
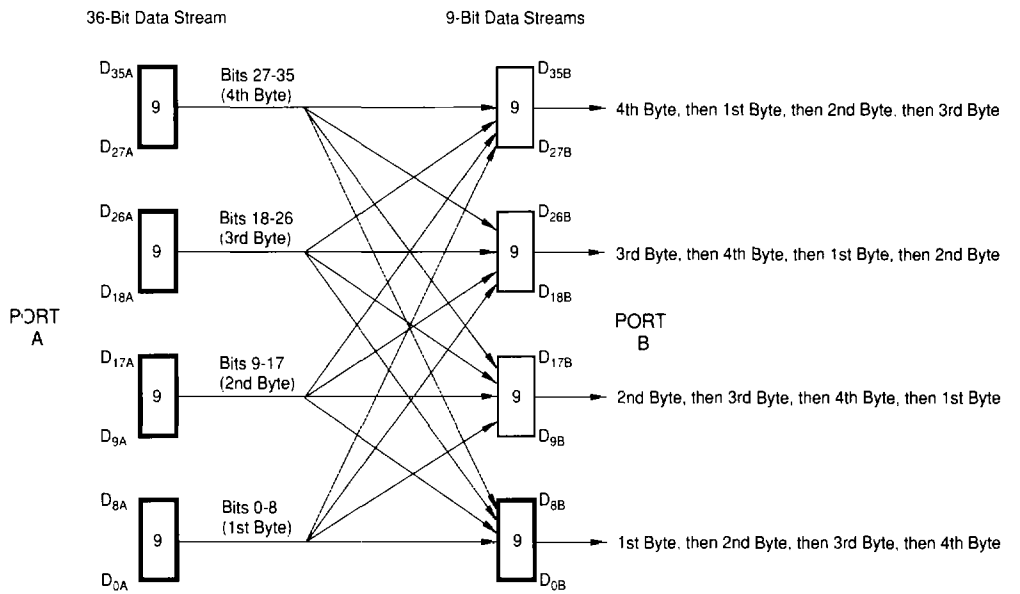


FIGURE 7B. 36-9 FUNNELING THROUGH FIFO #1



Notes:

1 The heavy black borders on the register segments indicate the main data path, suitable for most applications. Alternate paths feature a different ordering of bytes within a word, at Port B.

2 The funneling process does not change the ordering of bits within a byte. Halfwords (Figure 7A) or bytes (Figure 7B) are transferred in parallel form from Port A to Port B.

3 The word-width setting may be changed during system operation: however, two clock intervals should be allowed for these signals to settle before again attempting to read data D35-D0. Also, incomplete data words may occur when the word width is changed from shorter to longer at an inappropriate point in the data block passing through the FIFO.

FIGURE 8A. 18-TO-36 DEFUNNELING THROUGH FIFO #2

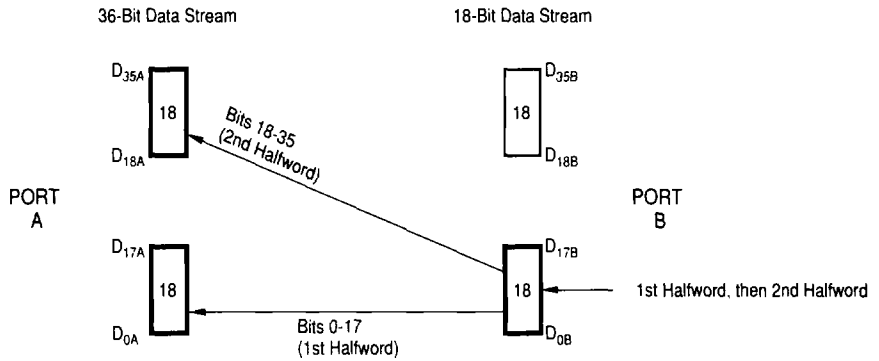
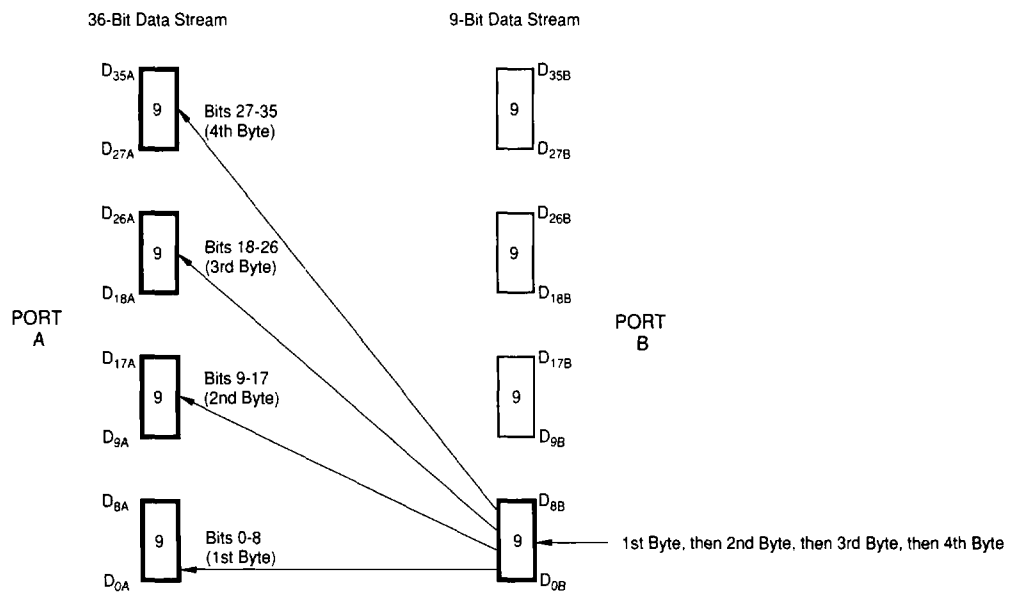


FIGURE 8B. 9-TO-36 DEFUNNELING THROUGH FIFO #2

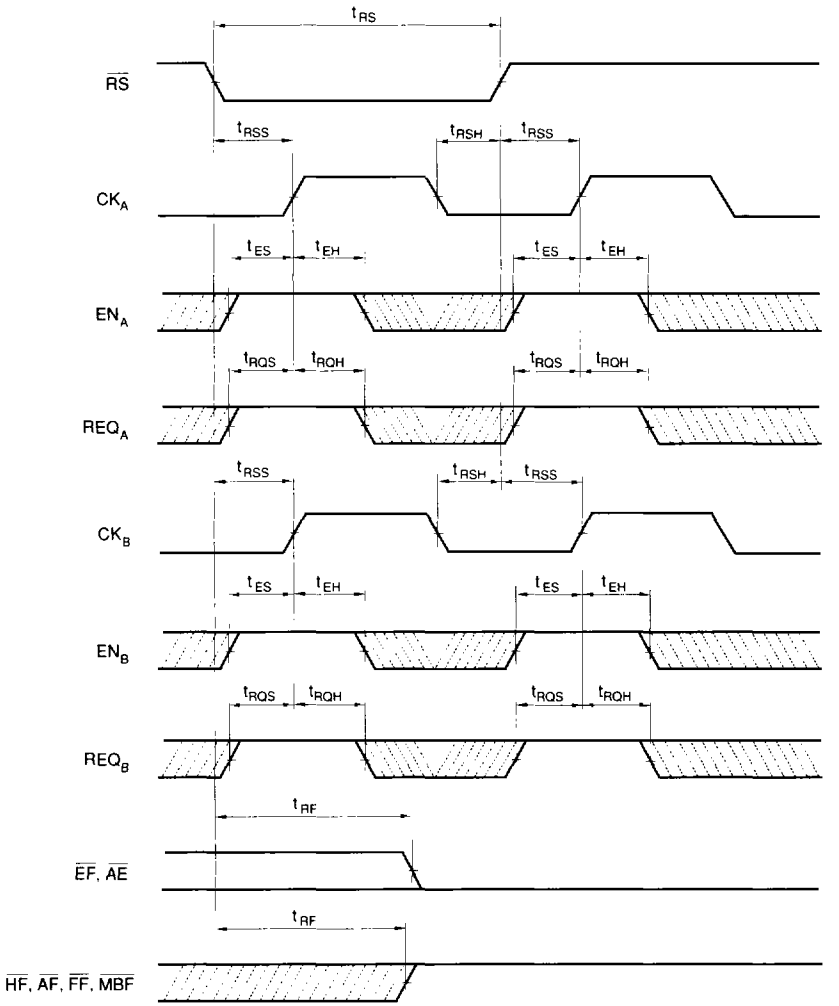


Notes:

1. The heavy black borders on the register segments indicate the only data paths used. The other byte seqments of Port B do not participate in the data path during defunneling.
2. The defunneling process does not change the ordering of bits within a byte. Halfwords (Figure 8A) or bytes (Figure 8B) are transferred in parallel form from Port A to Port B.
3. The word-width setting may be changed during system operation; however, two clock intervals should be allowed for these signals to settle before again attempting to send data. Also, incomplete data words may occur when the word width is changed from shorter to longer, at an inappropriate point in the data block passing through the FIFO.

TIMING DIAGRAMS

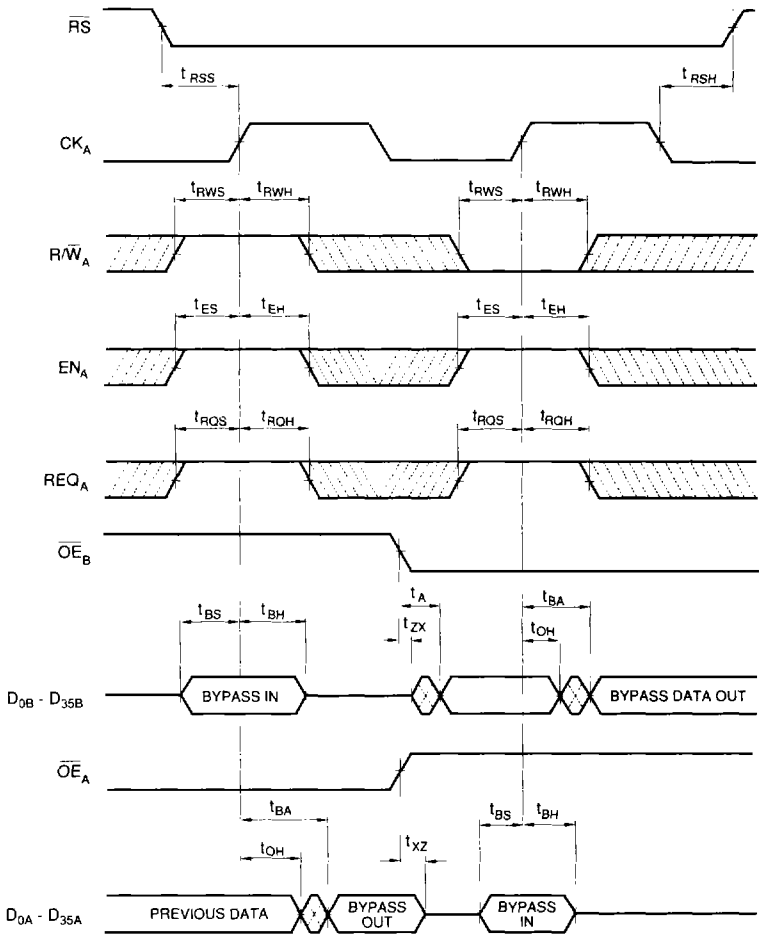
FIGURE 9. RESET TIMING



NOTES:

1. $\overline{RS}$ overrides all other input signals, except for $R/\overline{W}_A$, EN_A, and REQ_A. It operates asynchronously. $\overline{RS}$ operates whether or not EN_A and/or EN_B are asserted. However, at least one rising edge and one falling edge of both CK_A and CK_B must occur while $\overline{RS}$ is being asserted (is LOW), with timing as defined by t_{RSS} and t_{RSH}.
2. Otherwise, t_{RSS}, t_{RSH} need not be met unless the rising edge of CK_A and/or CK_B occurs while that clock is enabled.
3. The parity-check even/odd selection (Control Register bit 00) is initialized to odd byte parity at reset (HIGH). All other Control Register bits are initialized LOW.
4. The $\overline{AE}$ and $\overline{AF}$ flag offsets are initialized to eight locations from the boundary at reset.

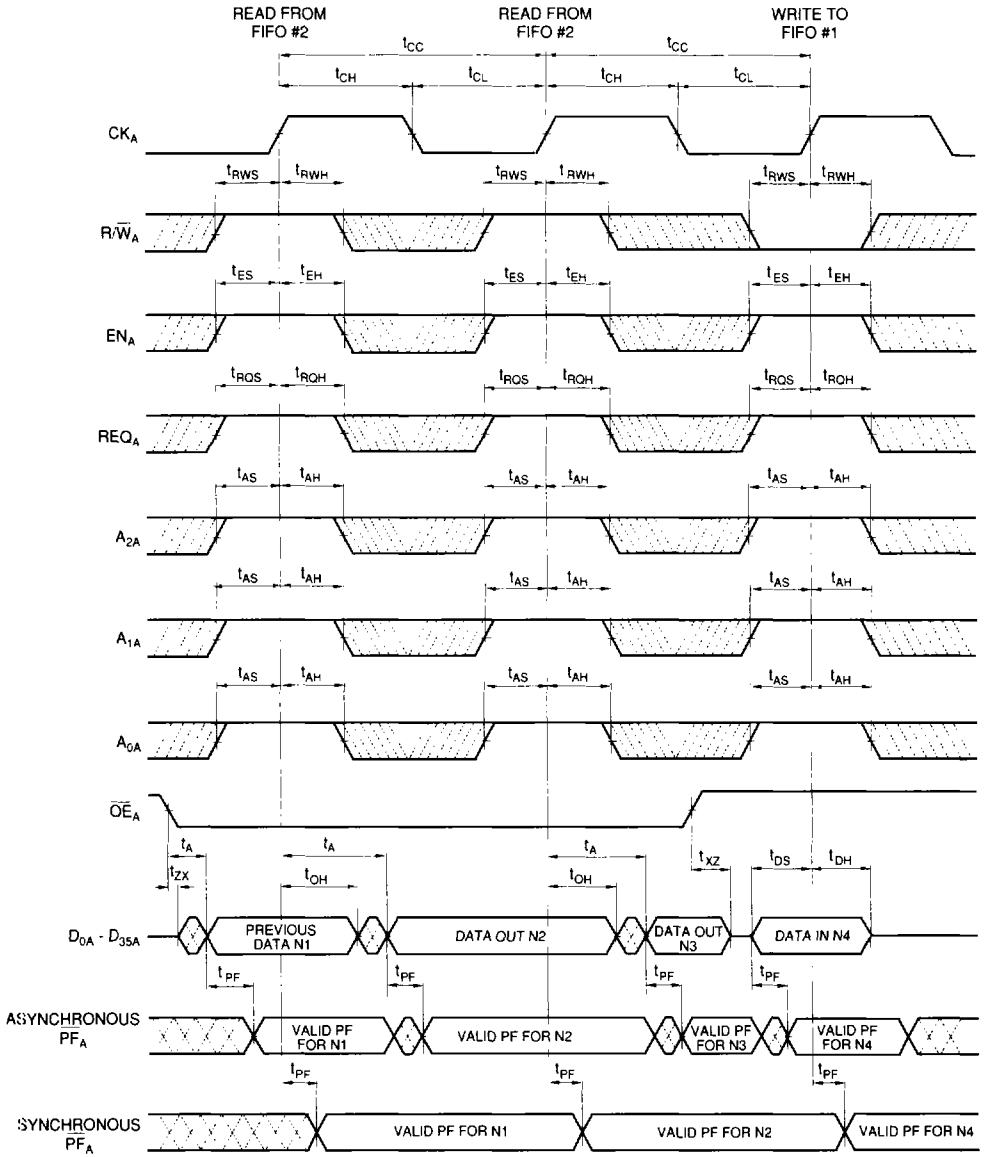
FIGURE 10. DATA BYPASS TIMING



NOTES:

1. t_{RSS}, t_{RSH} need not be met unless the rising edge of CK_A or CK_B occurs while that clock is enabled.
2. Port A is considered the master port for bypass operation. Thus, CK_A, $R/\overline{W}_A$, EN_A, and REQ_A control the transmission of data between ports at reset.

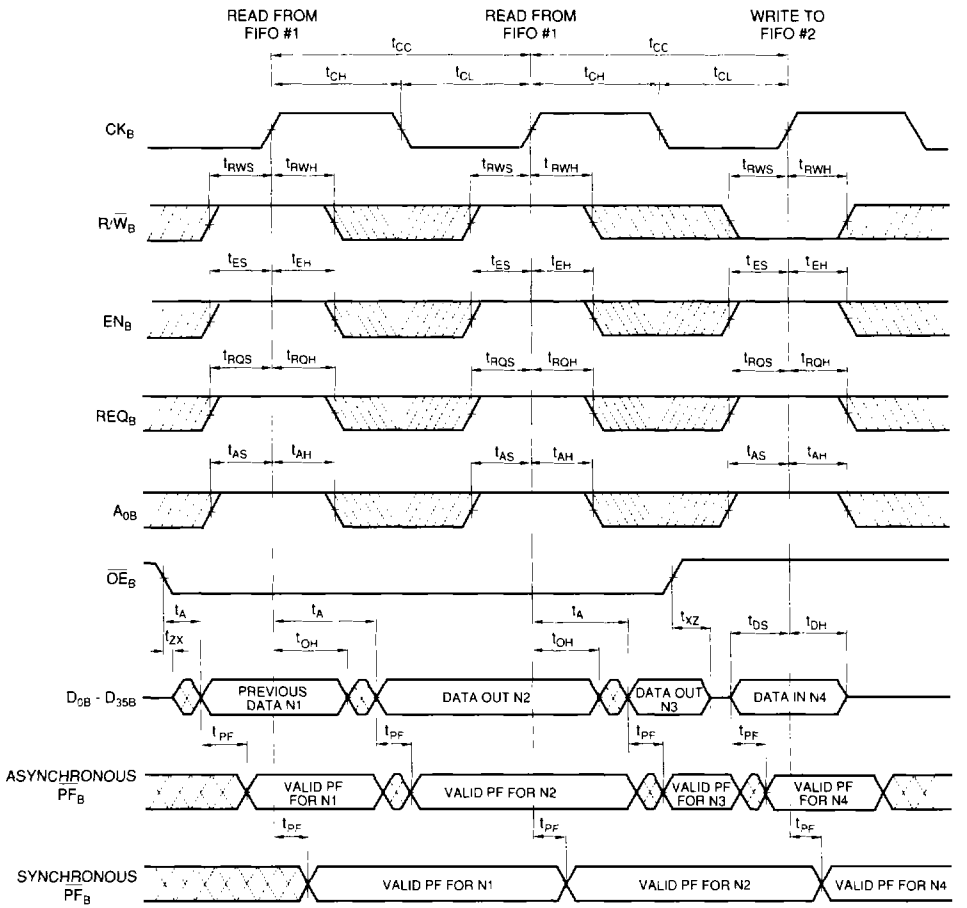
FIGURE 11. PORT A FIFO READ/WRITE



NOTES:

1. The Port A Parity Error Flag ($\overline{PF}_A$) reflects the parity status of data present on the data bus, after a delay t_{PF}, when operated asynchronously.
2. The Port A Parity Error Flag (PF_A) reflects the parity status of data present on the data bus during the previous clock cycle, and meeting the setup time at CK_A, when operated synchronously.
3. The status of $\overline{OE}_A$ does not gate read or write operations.
4. If $\overline{OE}_A$ is left LOW during a write operation, then the previous data held in the output latch is written back into FIFO #1.

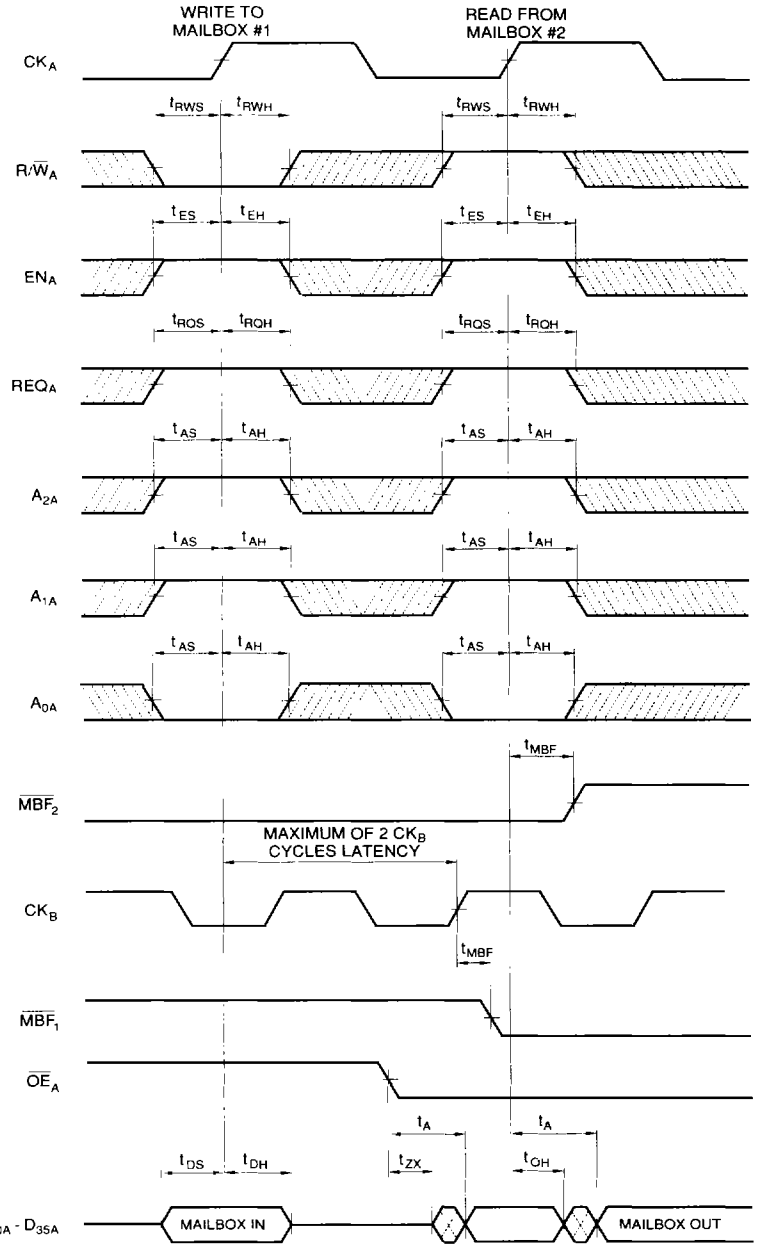
FIGURE 12. PORT B FIFO READ/WRITE



NOTES:

1. The Port B Parity Error Flag ($\overline{PF}_B$) reflects the parity status of data present on the data bus, after a delay t_{PF}, when operated asynchronously
2. The Port B Parity Error Flag (PF_B) reflects the parity status of data present on the data bus during the previous clock cycle, and meeting the setup time at CK_B, when operated synchronously.
3. The status of $\overline{OE}_B$ does not gate read or write operations.
4. If $\overline{OE}_B$ is left LOW during a write operation, then the previous data held in the output latch is written back into FIFO #2

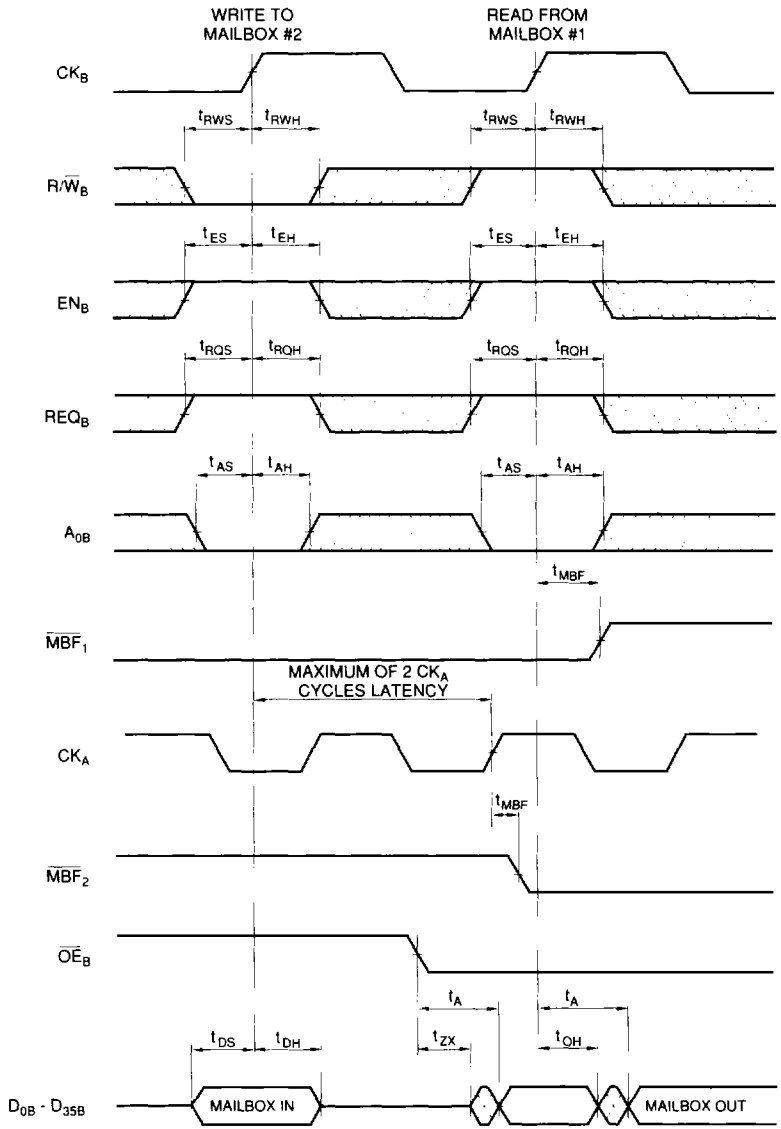
FIGURE 13. PORT A MAILBOX ACCESS



NOTES:

1. Both edges of $\overline{MBF}_2$ are synchronized to the Port A clock, CK_A.
2. Both edges of $\overline{MBF}_1$ are synchronized to the Port B clock, CK_B.
3. There is a maximum of two CK_B clock cycles of synchronization latency before $\overline{MBF}_1$ is asserted to indicate valid new mailbox data.
4. The status of mailbox flags does not prevent mailbox read or write operations.

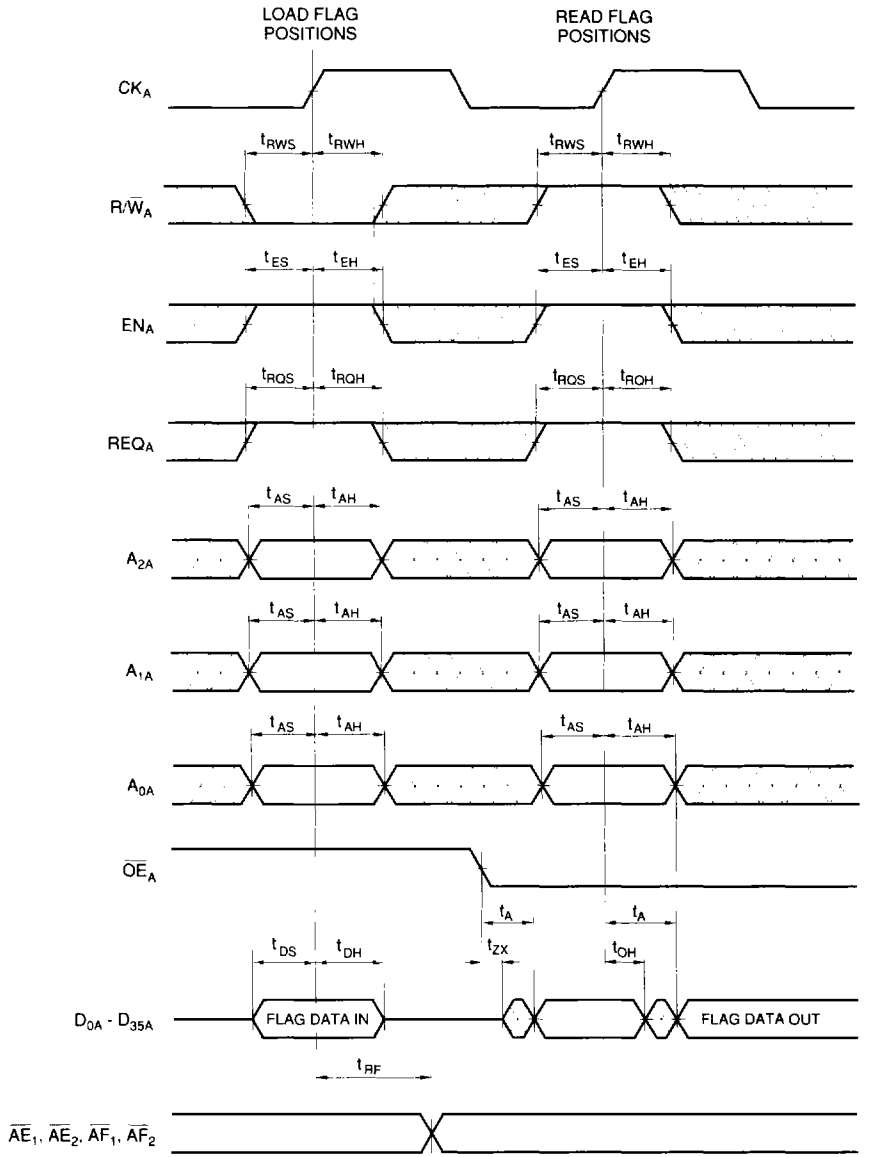
FIGURE 14. PORT B MAILBOX ACCESS



NOTES:

1. Both edges of $\overline{MBF}_2$ are synchronized to the Port A clock, CK_A.
2. Both edges of $\overline{MBF}_1$ are synchronized to the Port B clock, CK_B.
3. There is a maximum of two CK_A clock cycles of synchronization latency before MBF_2 is asserted to indicate valid new mailbox data.
4. The status of mailbox flags does not prevent mailbox read or write operations.

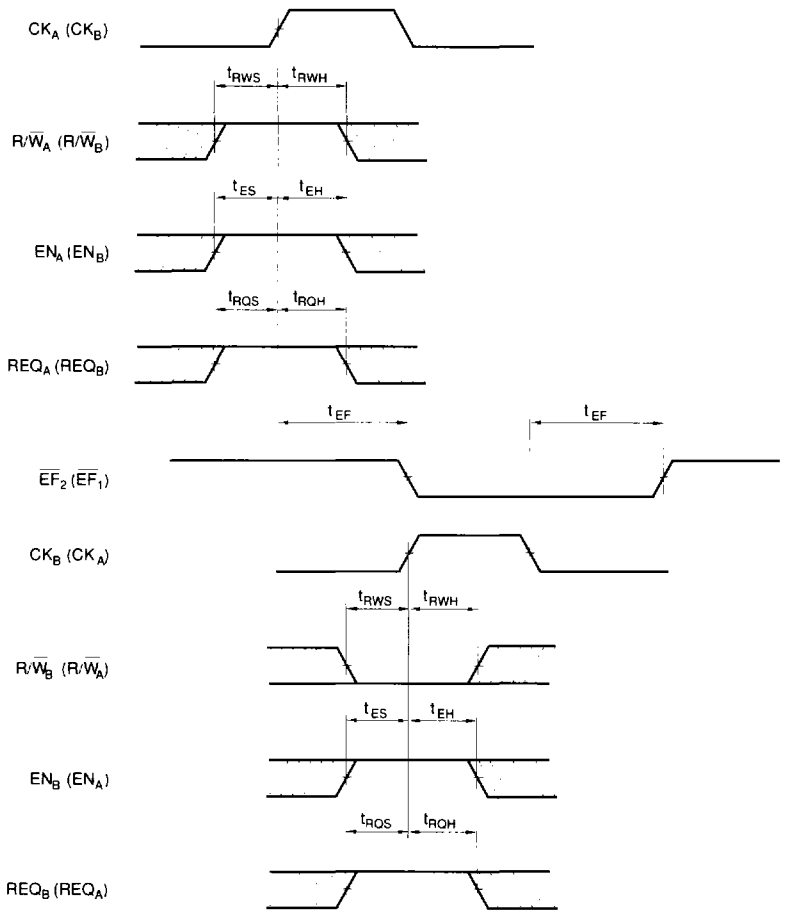
FIGURE 15. FLAG PROGRAMMING



NOTES:

1. For valid flag address codes and data formats, see Table 3.
2. If flag status is altered by flag programming, the updated flags will be valid within a time t_{RF}
3. The Control Register may be loaded or read back as shown here, with A_{2A}, A_{1A}, A_{0A} = HLL.

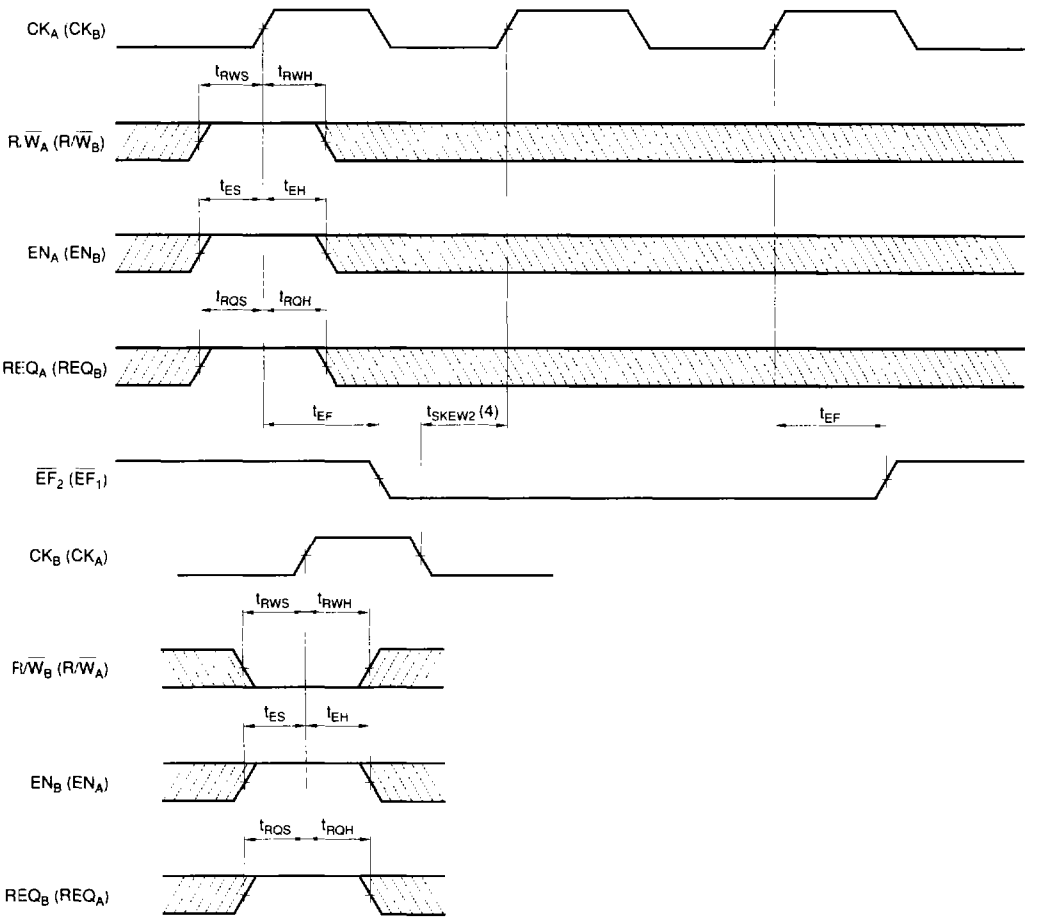
FIGURE 16. EMPTY FLAG TIMING, WHEN ASYNCHRONOUS



NOTES:

1. A_{2A}, A_{1A}, and A_{0A} all are held HIGH for FIFO access at Port A. A_{0B} is held HIGH for FIFO access at Port B.
2. Parameters without parentheses apply to FIFO #2 operation. Parameters with parentheses apply to FIFO #1 operation.
3. Assertion of the Empty Flags is controlled by rising clock edges; whereas, deassertion of the Empty Flags is controlled by falling clock edges.

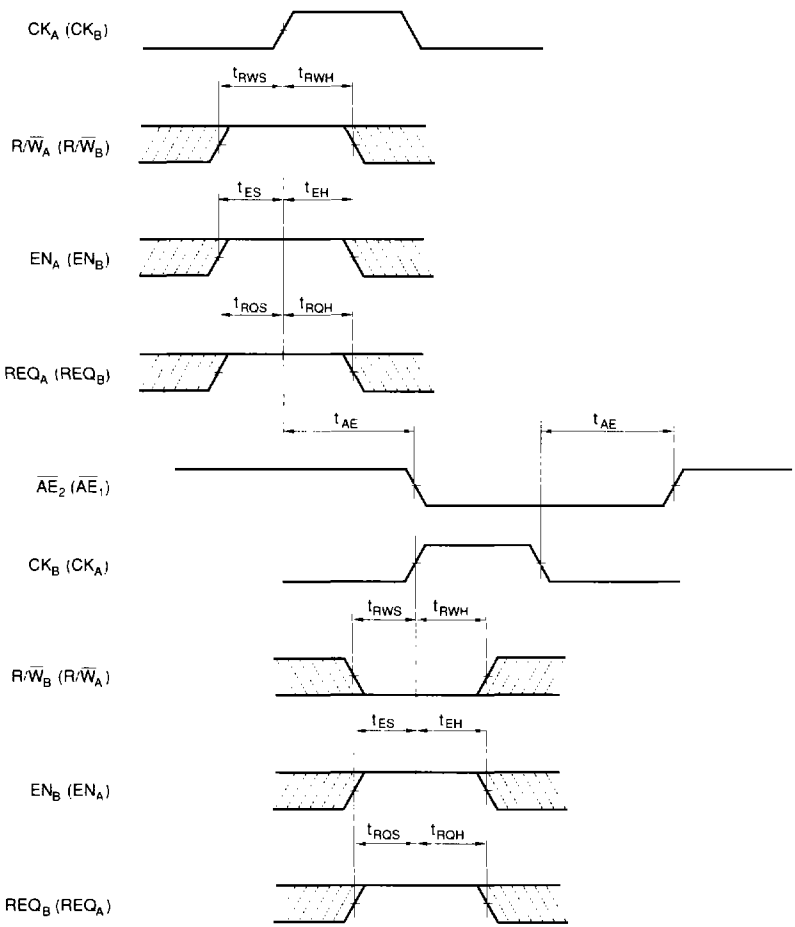
FIGURE 17. EMPTY FLAG TIMING, WHEN SYNCHRONOUS



NOTES:

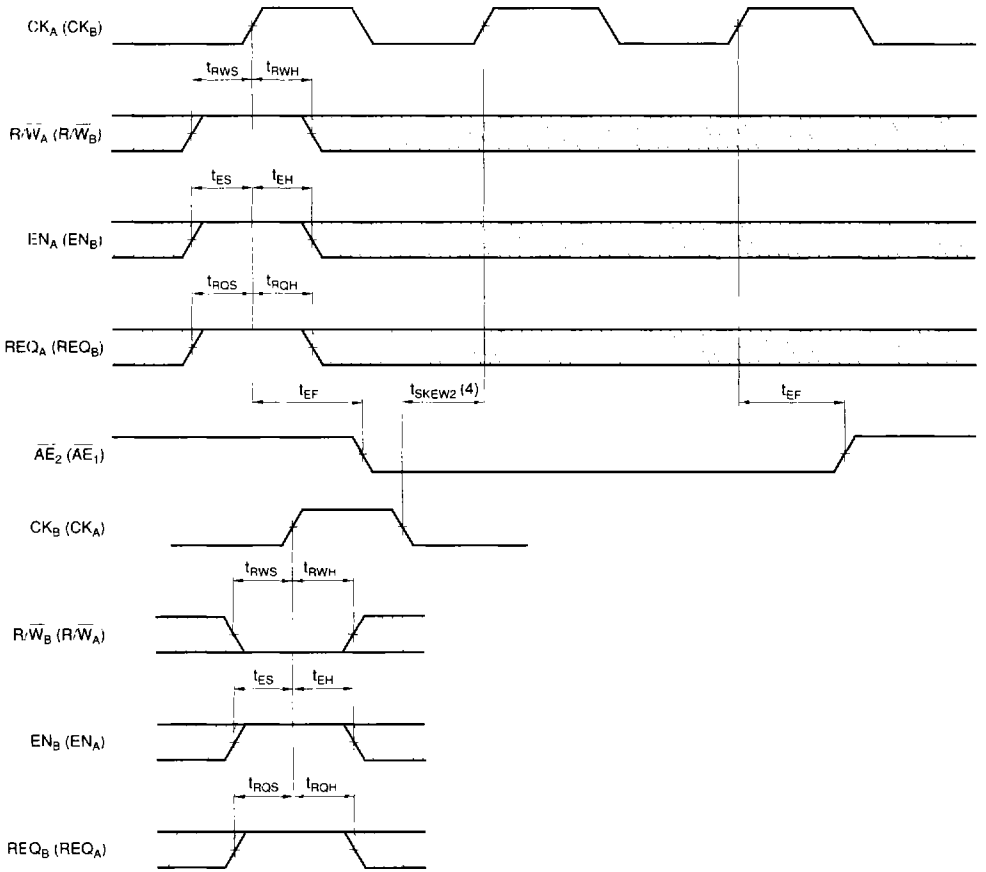
1. A_{2A}, A_{1A}, and A_{0A} all are held HIGH for FIFO access at Port A. A_{0B} is held HIGH for FIFO access at Port B.
2. Parameters without parentheses apply to FIFO #2 operation. Parameters with parentheses apply to FIFO #1 operation.
3. Assertion of the Empty Flags is controlled by rising clock edges; whereas, internal deassertion of the Empty Flags is controlled by falling clock edges, and their external deassertion is controlled by rising clock edges.
4. t_{SKEW2} is the minimum time between a falling CK_B (CK_A) edge and a rising CK_A (CK_B) edge for $\overline{EF}$ to change predictably during the current clock cycle. If the time between the falling edge of CK_B (CK_A) and the rising edge of CK_A (CK_B) is less than t_{SKEW2}, then it is not guaranteed that $\overline{EF}$ will change state until the next following CK_A (CK_B) edge.

FIGURE 18. ALMOST-EMPTY FLAG TIMING, WHEN ASYNCHRONOUS



NOTES:
1. A_{2A}, A_{1A}, and A_{0A} all are held HIGH for FIFO access at Port A. A_{0B} is held HIGH for FIFO access at Port B.
2. Parameters without parentheses apply to FIFO #2 operation. Parameters with parentheses apply to FIFO #1 operation.
3. Assertion of the Almost-Empty Flags is controlled by rising clock edges; whereas, deassertion of the Almost-Empty Flags is controlled by falling clock edges.

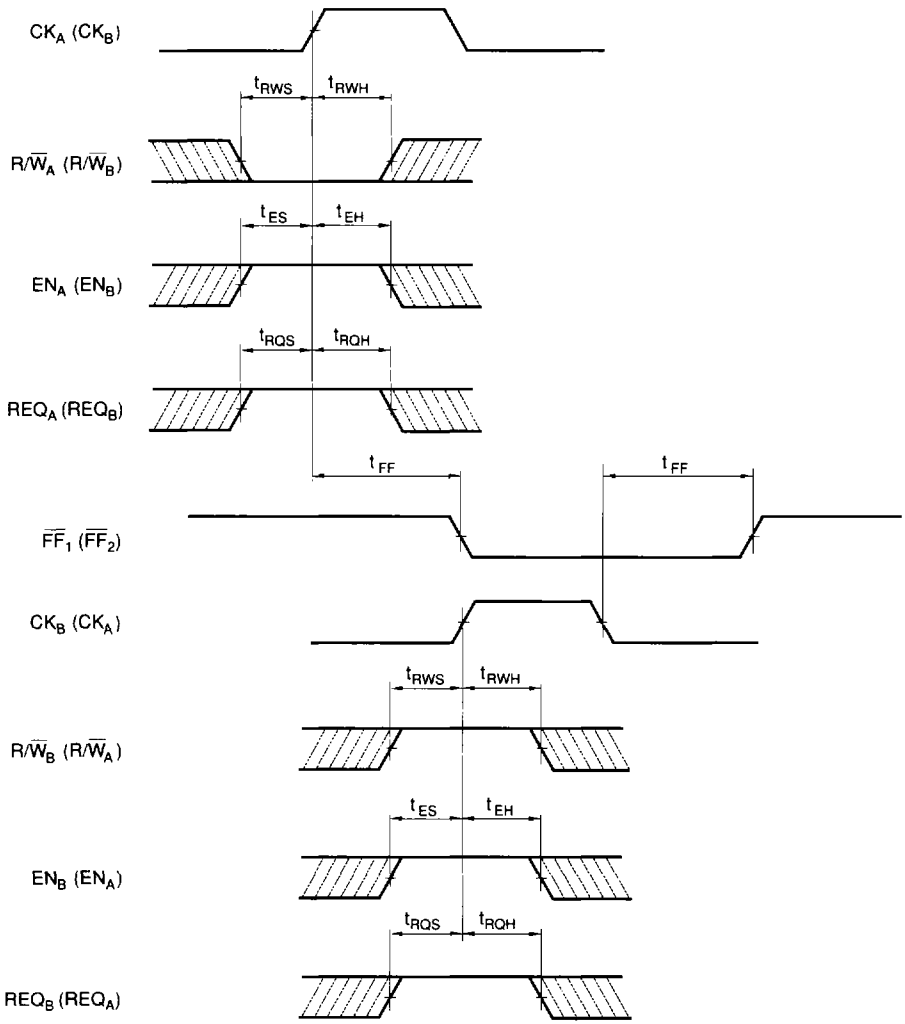
FIGURE 19. ALMOST-EMPTY FLAG TIMING, WHEN SYNCHRONOUS



NOTES:

1. A_{2A}, A_{1A}, and A_{0A} all are held HIGH for FIFO access at Port A. A_{0B} is held HIGH for FIFO access at Port B.
2. Parameters without parentheses apply to FIFO #2 operation. Parameters with parentheses apply to FIFO #1 operation.
3. Assertion of the Almost-Empty Flags is controlled by rising clock edges; whereas, internal deassertion of the Almost-Empty Flags is controlled by falling clock edges, and their external deassertion is controlled by rising clock edges.
4. t_{SKEW2} is the minimum time between a falling CK_B (CK_A) edge and a rising CK_A (CK_B) edge for $\overline{AE}$ to change predictably during the current clock cycle. If the time between the falling edge of CK_B (CK_A) and the rising edge of CK_A (CK_B) is less than t_{SKEW2}, then it is not guaranteed that $\overline{AE}$ will change state until the next following CK_A (CK_B) edge.

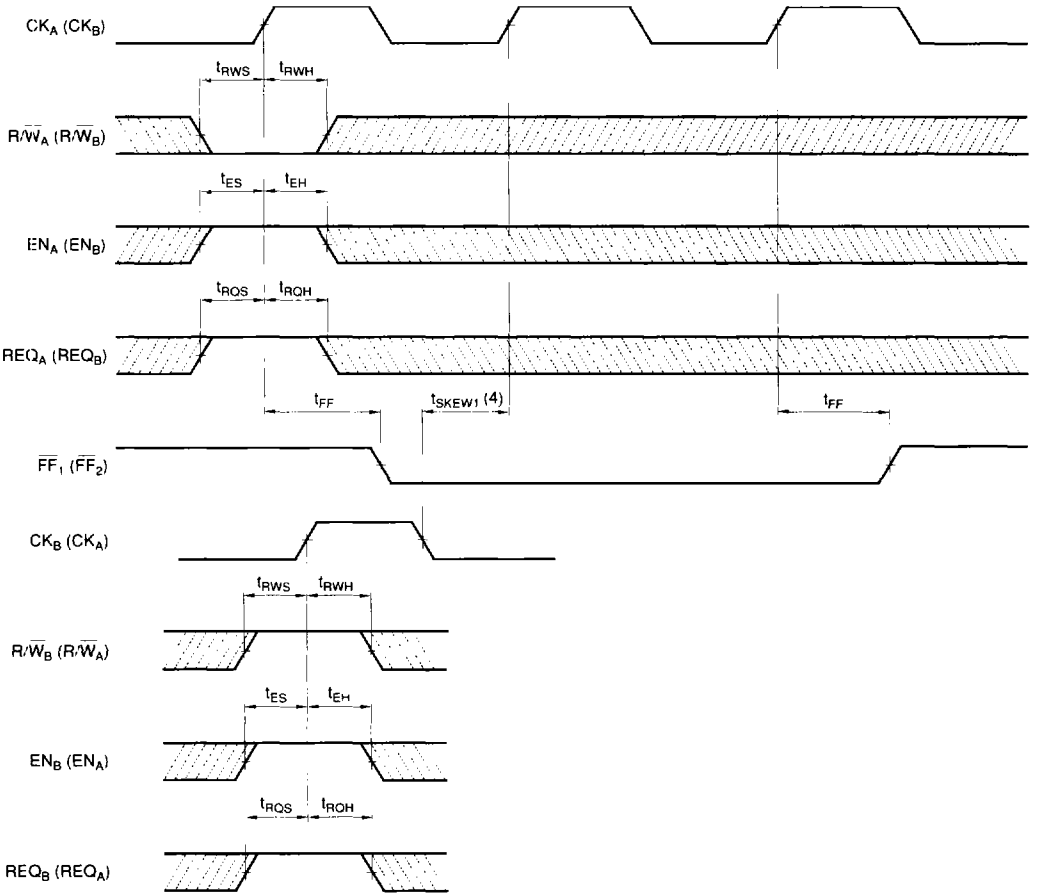
FIGURE 20. FULL FLAG TIMING, WHEN ASYNCHRONOUS



NOTES:

1. A_{2A}, A_{1A}, and A_{0A} all are held HIGH for FIFO access at Port A. A_{0B} is held HIGH for FIFO access at Port B.
2. Parameters without parentheses apply to FIFO #1 operation. Parameters with parentheses apply to FIFO #2 operation.
3. Assertion of the Full Flags is controlled by rising clock edges; whereas, deassertion of the Full Flags is controlled by falling clock edges.

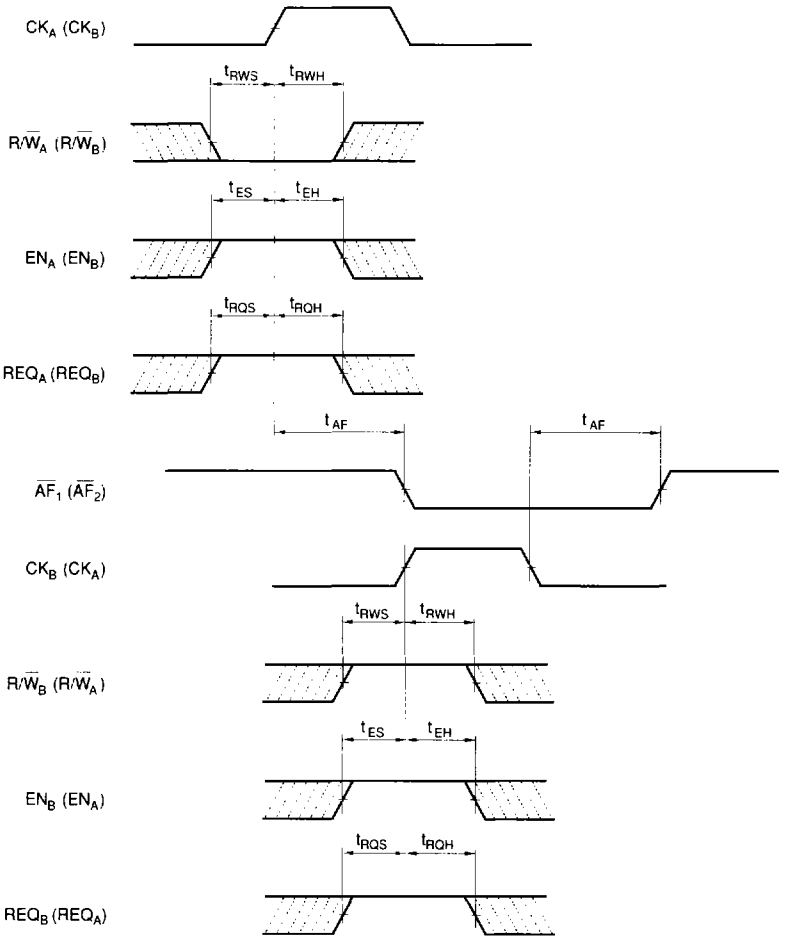
FIGURE 21. FULL FLAG TIMING, WHEN SYNCHRONOUS



NOTES:

1. A_{2A}, A_{1A}, and A_{0A} all are held HIGH for FIFO access at Port A. A_{0B} is held HIGH for FIFO access at Port B.
2. Parameters without parentheses apply to FIFO #1 operation. Parameters with parentheses apply to FIFO #2 operation.
3. Assertion of the Full Flags is controlled by rising clock edges; whereas, internal deassertion of the Full Flags is controlled by falling clock edges, and their external deassertion is controlled by rising clock edges.
4. t_{SKEW1} is the minimum time between a falling CK_B (CK_A) edge and a rising CK_A (CK_B) edge for $\overline{FF}$ to change predictably during the current clock cycle. If the time between the falling edge of CK_B (CK_A) and the rising edge of CK_A (CK_B) is less than t_{SKEW1}, then it is not guaranteed that $\overline{FF}$ will change state until the next following CK_A (CK_B) edge.

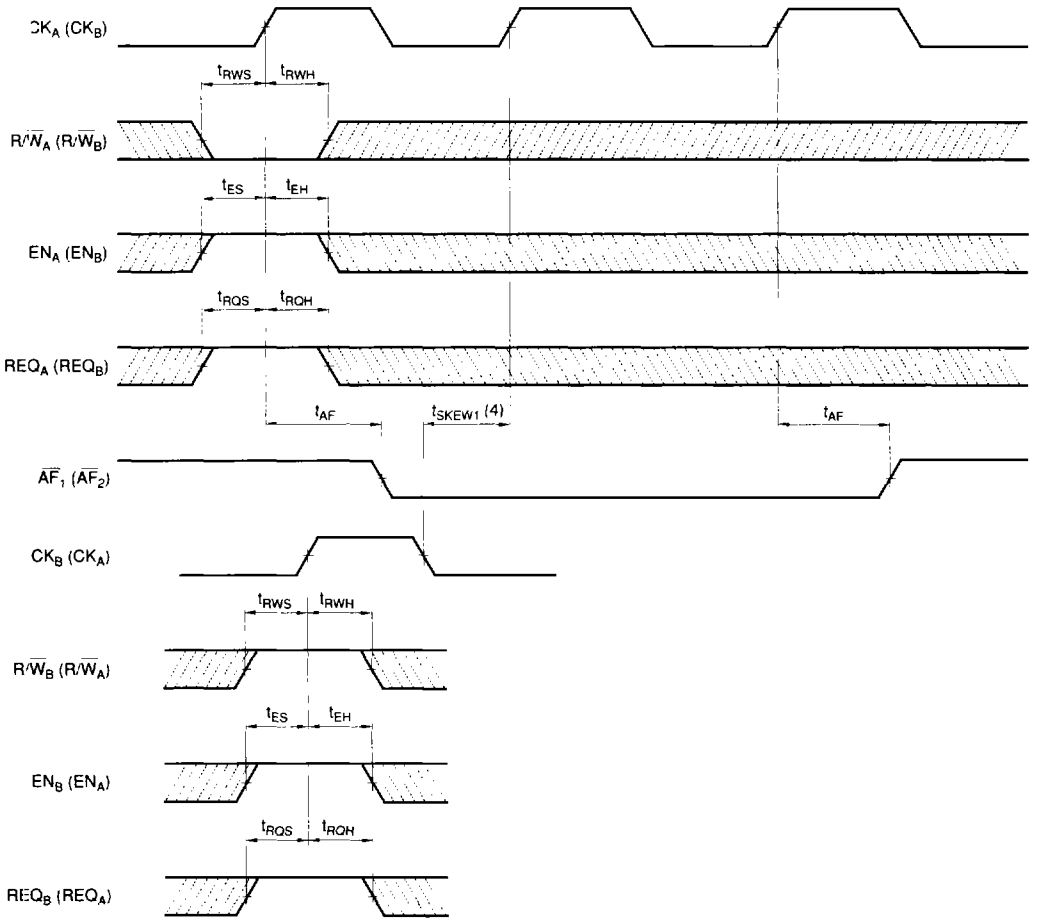
FIGURE 22. ALMOST-FULL FLAG TIMING, WHEN ASYNCHRONOUS



NOTES:

1. A_{2A}, A_{1A}, and A_{0A} all are held HIGH for FIFO access at Port A. A_{0B} is held HIGH for FIFO access at Port B.
2. Parameters without parentheses apply to FIFO #1 operation. Parameters with parentheses apply to FIFO #2 operation.
3. Assertion of the Almost-Full Flags is controlled by rising clock edges; whereas, deassertion of the Almost-Full Flags is controlled by falling clock edges.

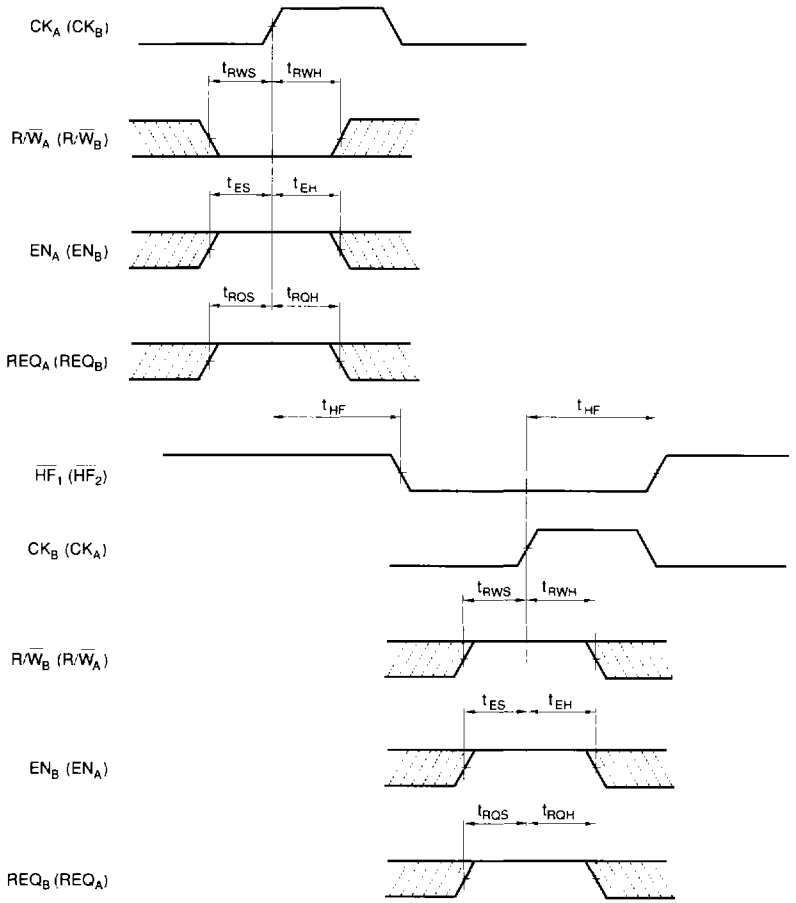
FIGURE 23. ALMOST-FULL FLAG TIMING, WHEN SYNCHRONOUS



NOTES:

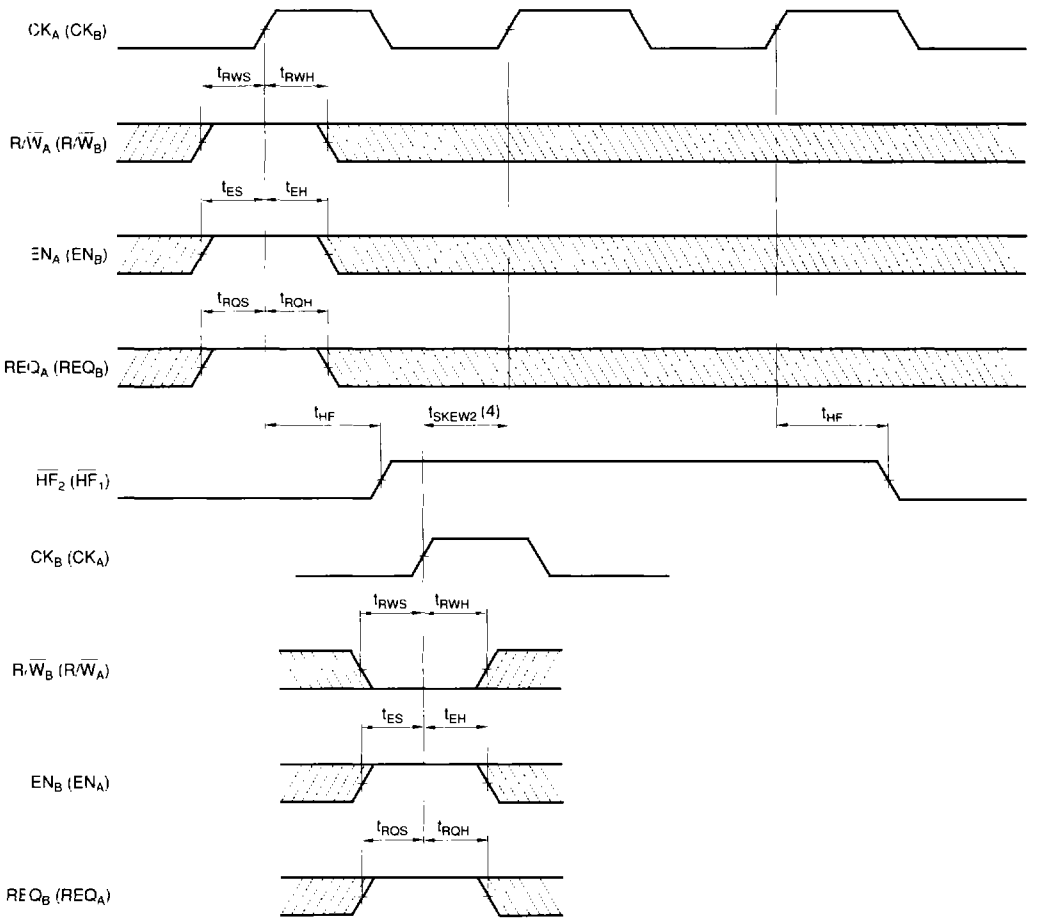
1. A_{2A}, A_{1A}, and A_{0A} all are held HIGH for FIFO access at Port A. A_{0B} is held HIGH for FIFO access at Port B.
2. Parameters without parentheses apply to FIFO #1 operation. Parameters with parentheses apply to FIFO #2 operation.
3. Assertion of the Almost-Full Flags is controlled by rising clock edges; whereas, internal deassertion of the Almost-Full Flags is controlled by falling clock edges, and their external deassertion is controlled by rising clock edges.
4. t_{SKEW1} *is the minimum time between a falling* CK_B (CK_A) *edge* and a rising CK_A (CK_B) edge for $\overline{AF}$ to change predictably during the current clock cycle. If the time between the falling edge of CK_B (CK_A) and the rising edge of CK_A (CK_B) is less than t_{SKEW1}, then it is not guaranteed that $\overline{AF}$ will change state until the next following CK_A (CK_B) edge.

FIGURE 24. HALF-FULL FLAG TIMING, WHEN ASYNCHRONOUS



NOTES:
1. A_{2A}, A_{1A}, and A_{0A} all are held HIGH for FIFO access at Port A. A_{0B} is held HIGH for FIFO access at Port B.
2. Parameters without parentheses apply to FIFO #1 operation. Parameters with parentheses apply to FIFO #2 operation.
3. Both assertion and deassertion of the Half-Full Flags are controlled entirely by rising clock edges, rather than by falling clock edges.

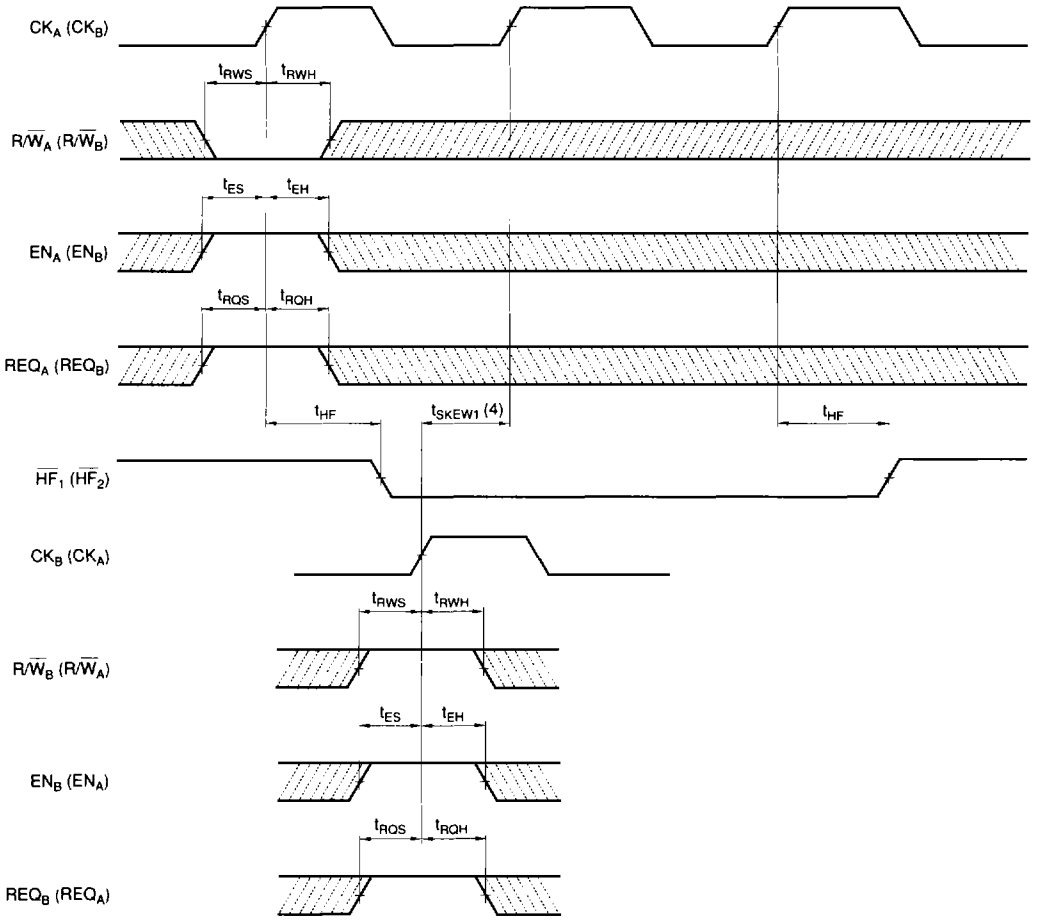
FIGURE 25. HALF-FULL FLAG TIMING, WHEN SYNCHRONIZED TO A PORT CLOCK DOING READING



NOTES:

1. A_{2A}, A_{1A}, and A_{0A} all are held HIGH for FIFO access at Port A. A_{0B} is held HIGH for FIFO access at Port B.
2. Parameters without parentheses apply to FIFO #2 operation. Parameters with parentheses apply to FIFO #1 operation.
3. Both assertion and deassertion of the Half-Full Flags are controlled entirely by rising clock edges, rather than by falling clock edges.
4. t_{SKEW2} is the minimum time between a falling CK_B (CK_A) edge and a rising CK_A (CK_B) edge for $\overline{HF}$ to change predictably during the current clock cycle. If the time between the falling edge of CK_B (CK_A) and the rising edge of CK_A (CK_B) is less than t_{SKEW2}, then it is not guaranteed that $\overline{HF}$ will change state until the next following CK_A (CK_B) edge.

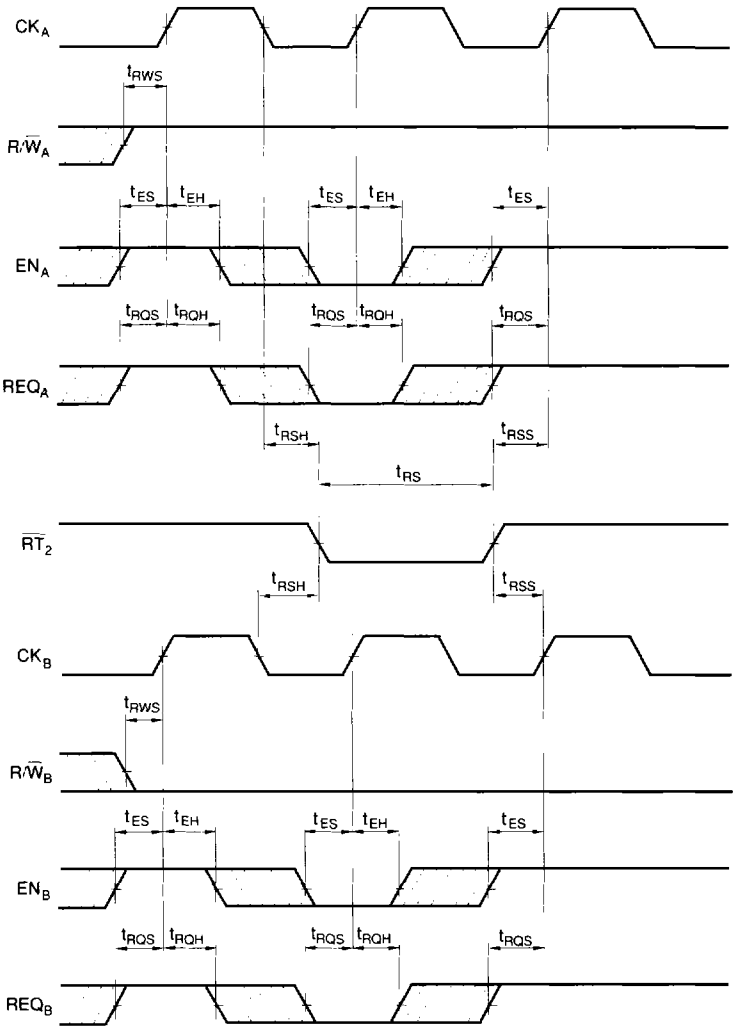
FIGURE 26. HALF-FULL FLAG TIMING, WHEN SYNCHRONIZED TO A PORT CLOCK DOING WRITING



NOTES:

1. A_{2A}, A_{1A}, and A_{0A} all are held HIGH for FIFO access at Port A. A_{0B} is held HIGH for FIFO access at Port B.
2. Parameters without parentheses apply to FIFO #1 operation. Parameters with parentheses apply to FIFO #2 operation.
3. Both assertion and deassertion of the Half-Full Flags are controlled entirely by rising clock edges, rather than by falling clock edges.
4. t_{SKEW1} is the minimum time between a falling CK_B (CK_A) edge and a rising CK_A (CK_B) edge for $\overline{HF}$ to change predictably during the current clock cycle. If the time between the falling edge of CK_B (CK_A) and the rising edge of CK_A (CK_B) is less than t_{SKEW1}, then it is not guaranteed that $\overline{HF}$ will change state until the next following CK_A (CK_B) edge.

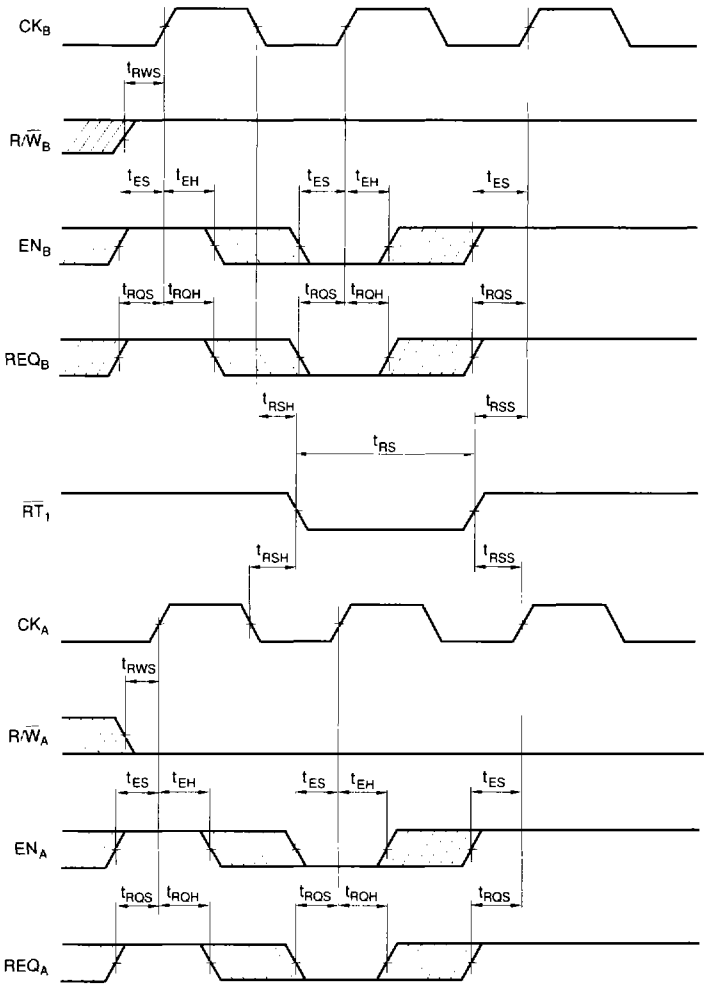
FIGURE 27. FIFO #2 RETRANSMIT TIMING



NOTES:

1. t_{RSS} and t_{RSH} need not be met unless a rising edge of CK_A or CK_B occurs while that clock is enabled.
2. t_{RSS} is the time needed to deassert $\overline{RT}_2$ before returning to a normal FIFO cycle.
3. t_{RSH} is the time needed before asserting $\overline{RT}_2$ after a normal FIFO cycle.
4. Read and write operations to FIFO #2 should be disabled while $\overline{RT}_2$ is being asserted.

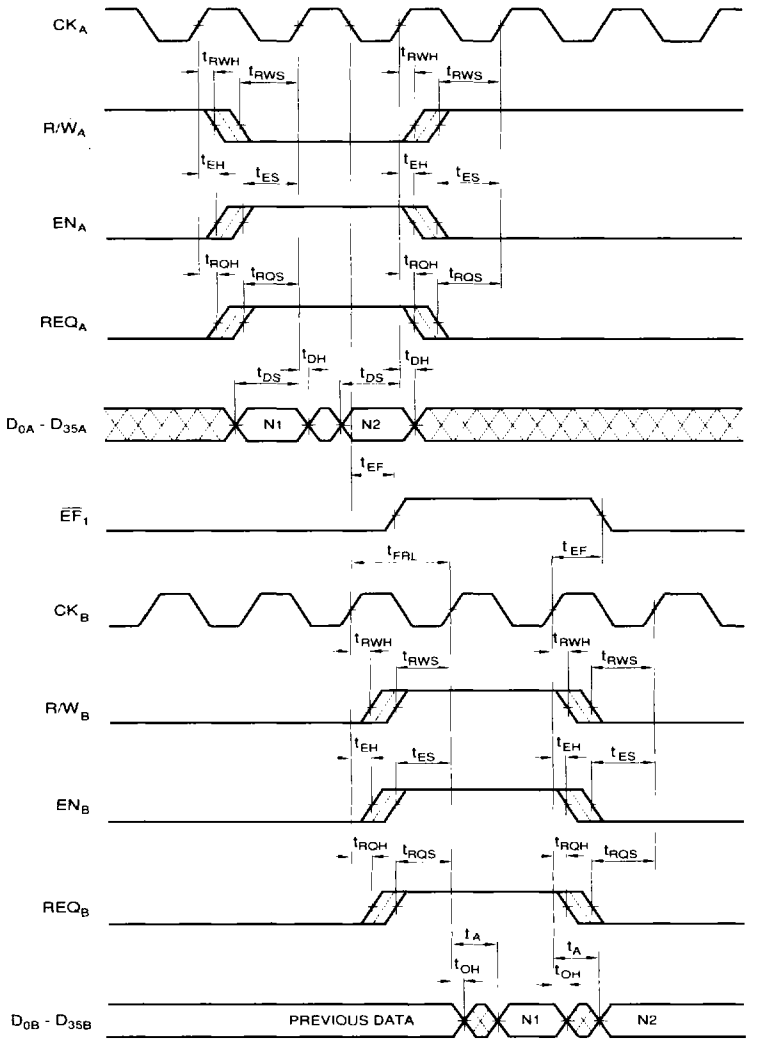
FIGURE 28. FIFO #1 RETRANSMIT TIMING



NOTES:

1. t_{RSS} and t_{RSH} need not be met unless a rising edge of CK_A or CK_B occurs while that clock is enabled.
2. t_{RSS} is the time needed to deassert $\overline{RT}_1$ before returning to a normal FIFO cycle.
3. t_{RSH} is the time needed before asserting $\overline{RT}_1$ after a normal FIFO cycle.
4. Read and write operations to FIFO #1 should be disabled while $\overline{RT}_1$ is being asserted.

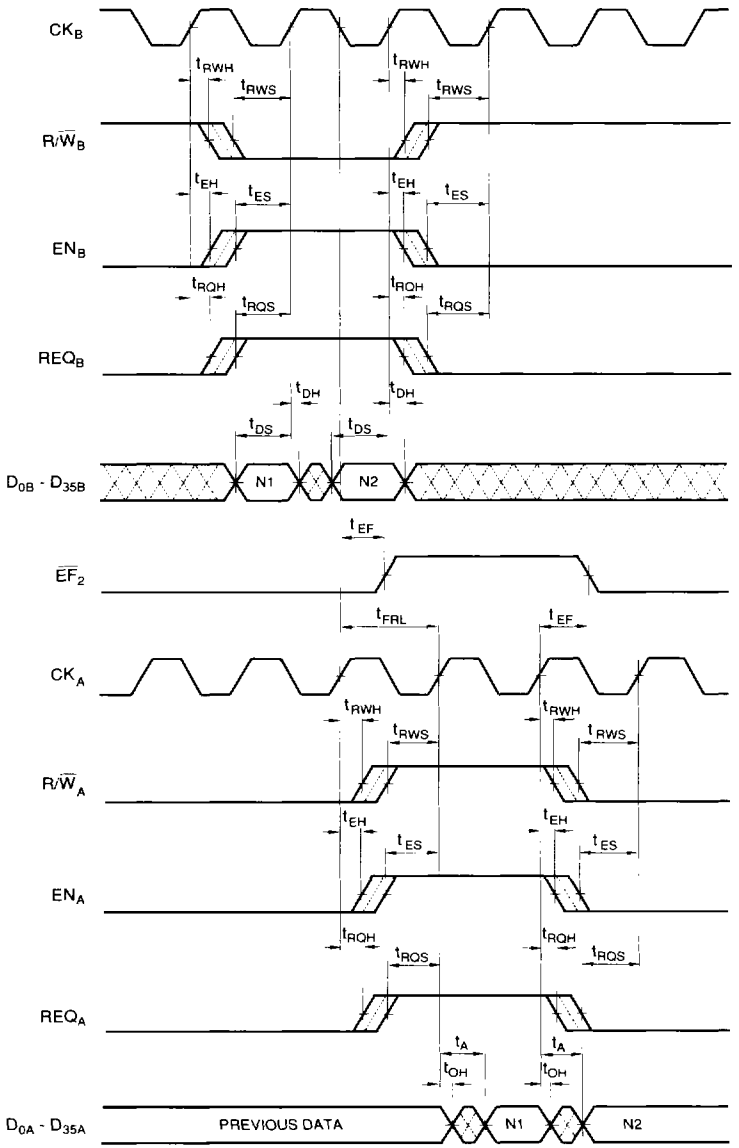
FIGURE 29. FIFO #1 WRITE AND READ OPERATION IN NEAR-EMPTY REGION



NOTES:

1. A_{2A}, A_{1A}, A_{0A}, and A_{0B} are all held HIGH for FIFO access.
2. $\overline{OE}_A$ is held HIGH.
3. $\overline{OE}_B$ is held LOW.
4. t_{FRL} (First Read Latency) - The first read following an empty condition may begin no earlier than t_{FRL} after the first write to an empty FIFO, to ensure that valid read data is retrieved.

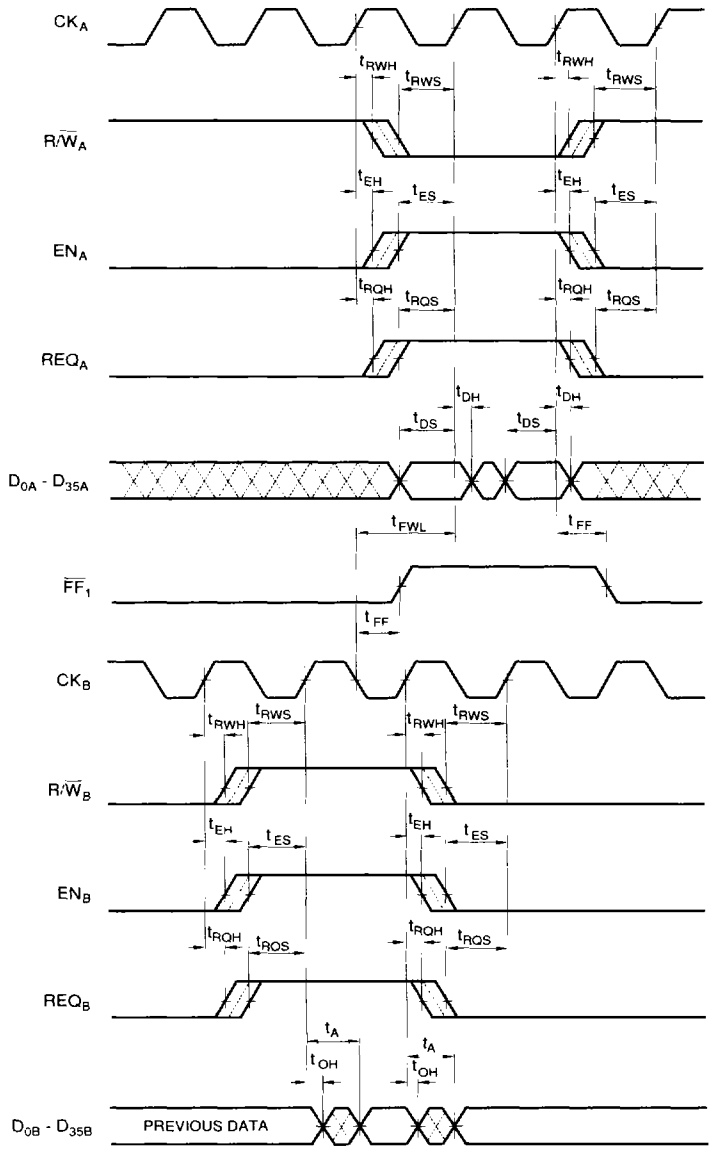
FIGURE 30. FIFO #2 WRITE AND READ OPERATION IN NEAR-EMPTY REGION



NOTES:

1. A_{2A}, A_{1A}, A_{0A}, and A_{0B} are all held HIGH for FIFO access.
2. $\overline{OE}_B$ is held HIGH.
3. $\overline{OE}_A$ is held LOW.
4. t_{FRL} (First Read Latency) - The first read following an empty condition may begin no earlier than t_{FRL} after the first write to an empty FIFO, to ensure that valid read data is retrieved.

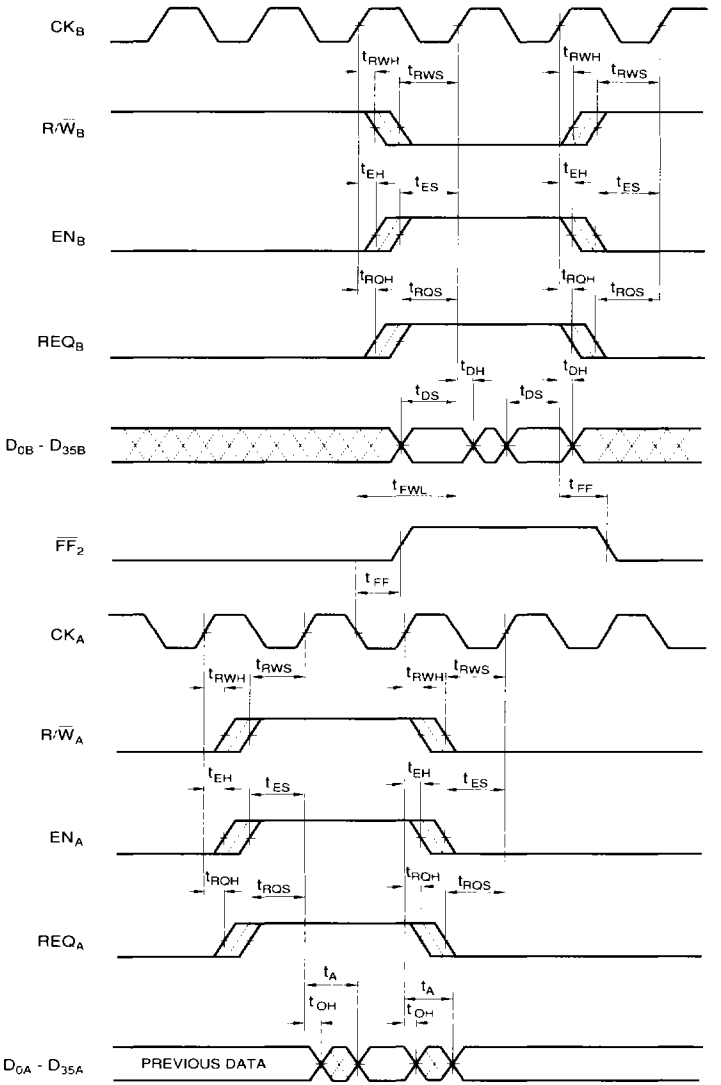
FIGURE 31. FIFO #1 READ AND WRITE OPERATION IN NEAR-FULL REGION



NOTES:

1. A_{2A}, A_{1A}, and A_{0A} all are held HIGH for FIFO access at Port A. $\overline{A_{0B}}$ is held HIGH for FIFO access at Port B.
2. $\overline{OE}_A$ is held HIGH.
3. $\overline{OE}_B$ is held LOW.
4. t_{FWL} (First Write Latency) - The first write following a full condition may begin no earlier than t_{FWL} after the first read from a full FIFO, to ensure that valid write data is written.

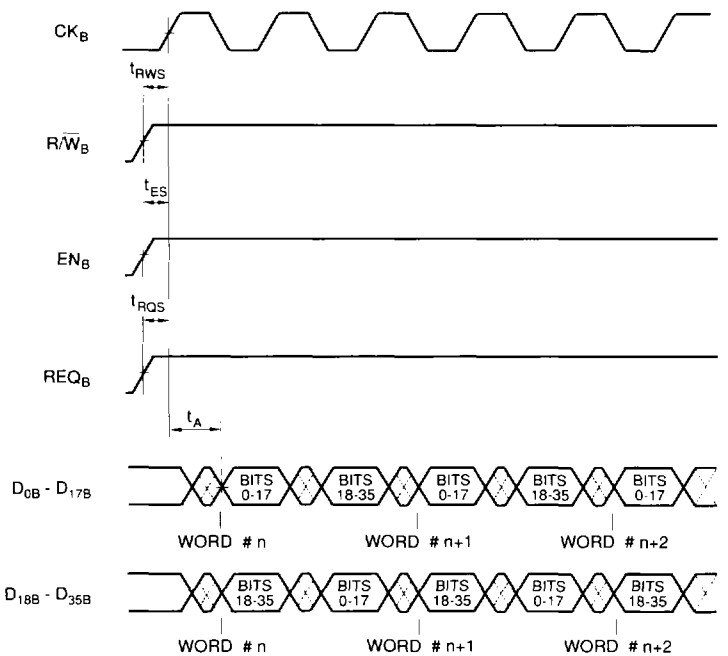
FIGURE 32. FIFO #2 READ AND WRITE OPERATION IN NEAR-FULL REGION



NOTES:

1. A_{2A}, A_{1A}, and A_{0A} all are held HIGH for FIFO access at Port A. A_{0B} is held HIGH for FIFO access at Port B.
2. $\overline{OE}_B$ is held HIGH.
3. $\overline{OE}_A$ is held LOW.
4. t_{FWL} (First Write Latency) - The first write following a full condition may begin no earlier than t_{FWL} after the first read from a full FIFO. to ensure that valid write data is written.

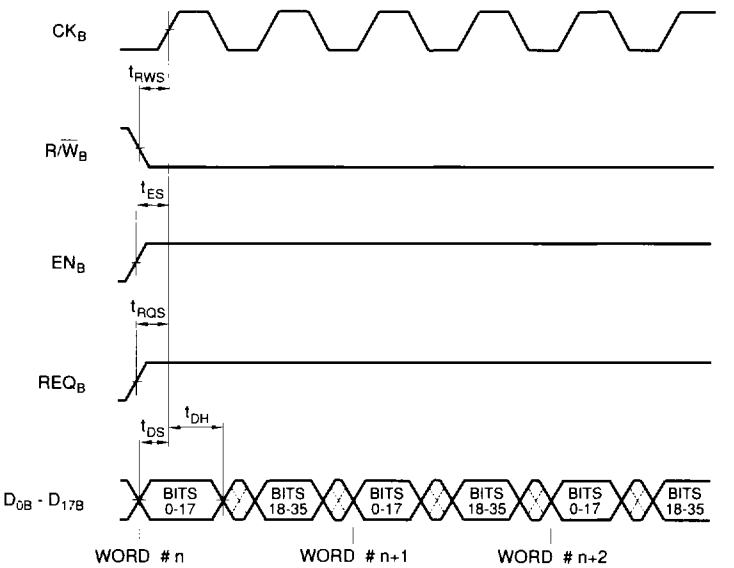
FIGURE 33. PORT B DOUBLE-BYTE FIFO #1 READ ACCESS FOR 36-TO-18 FUNNELING



NOTES:

1. A_{0B} is held HIGH for FIFO access.
2. $\overline{OE}_B$ is held LOW.
3. $\overline{WS}_0$ is held HIGH and WS_1 is held LOW for double-byte access.
4. Data-access time t_A, after the rising edge of CK_B, shown for the first read cycle, applies similarly for all subsequent read cycles.

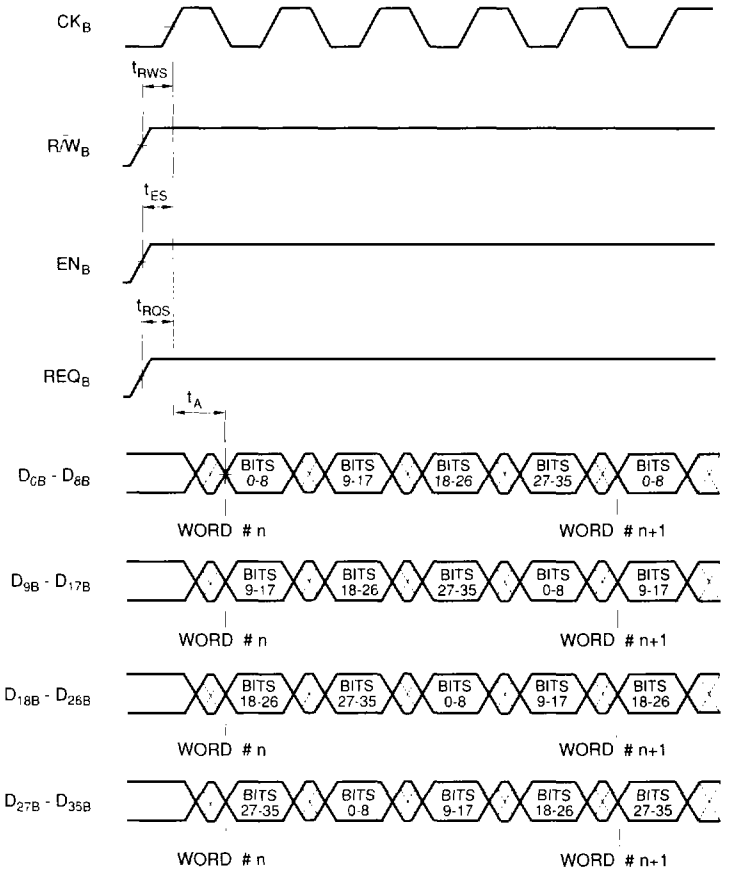
FIGURE 34. DOUBLE-BYTE FIFO #2 WRITE ACCESS FOR 18-TO-36 DEFUNNELING



NOTES:

1. $\overline{A_{0B}}$ is held HIGH for FIFO access.
2. $\overline{OE_B}$ is held HIGH.
3. WS_0 is held HIGH and WS_1 is held LOW for double-byte access.
4. Data-setup time t_{DS} and data-hold time t_{DH}, before and after the rising edge of CK_B, shown for the first write cycle, apply similarly for all subsequent write cycles.

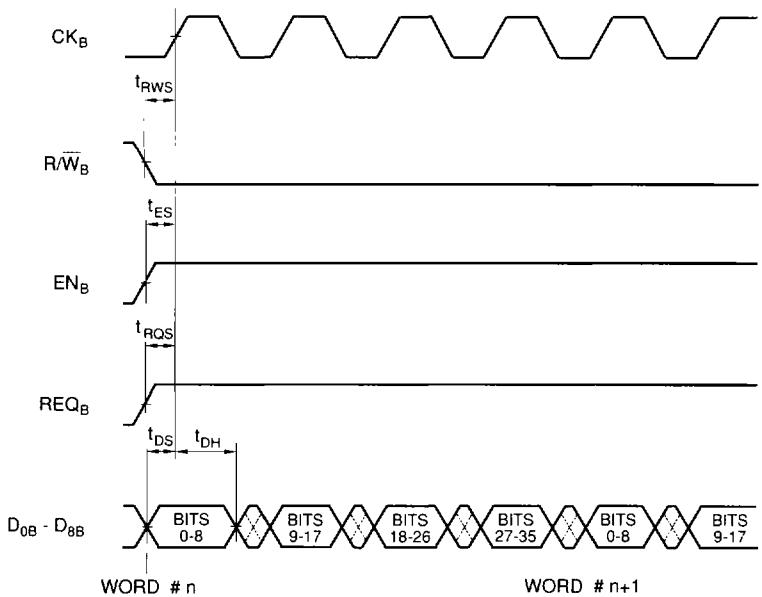
FIGURE 35. PORT B SINGLE-BYTE FIFO #1 READ ACCESS FOR 36-TO-9 FUNNELING



NOTES:

1. A_{0B} is held HIGH for FIFO access.
2. $\overline{OE}_B$ is held LOW.
3. WS_0 *and* WS_1 *both are held LOW for single-byte access.*
4. Data-access time t_A, after the rising edge of CK_B, shown for the first read cycle. applies similarly for all subsequent read cycles.

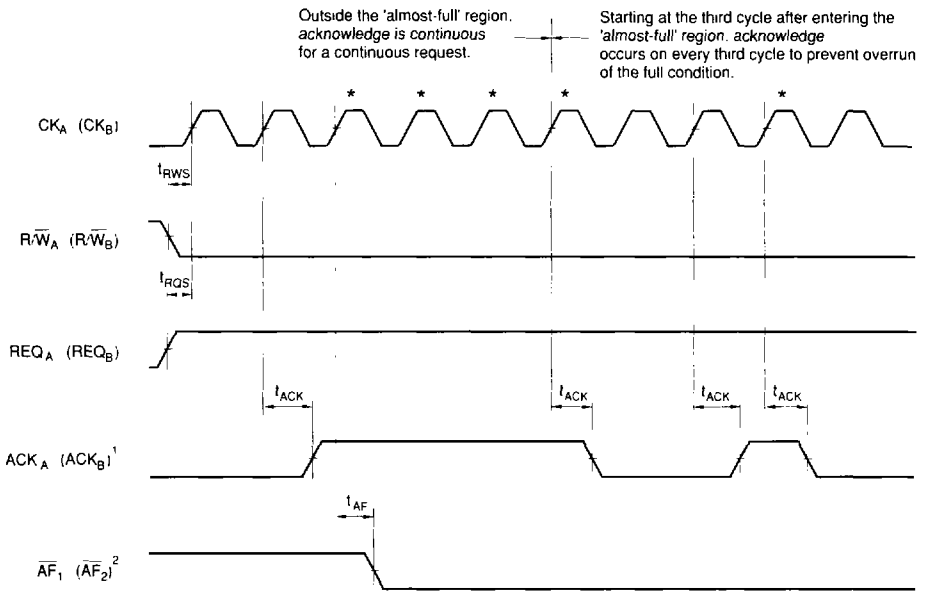
FIGURE 36. PORT B SINGLE-BYTE FIFO #2 WRITE ACCESS FOR 9-TO-36 DEFUNNELING



NOTES:

1. A_{0B} is held HIGH for FIFO access.
2. $\overline{OE}_B$ is held HIGH.
3. WS_0 and WS_1 both are held LOW for single-byte access.
4. Data-setup time t_{DS} and data-hold time t_{DH}, before and after the rising edge of CK_B, shown for the first write cycle. apply similarly for all subsequent write cycles.

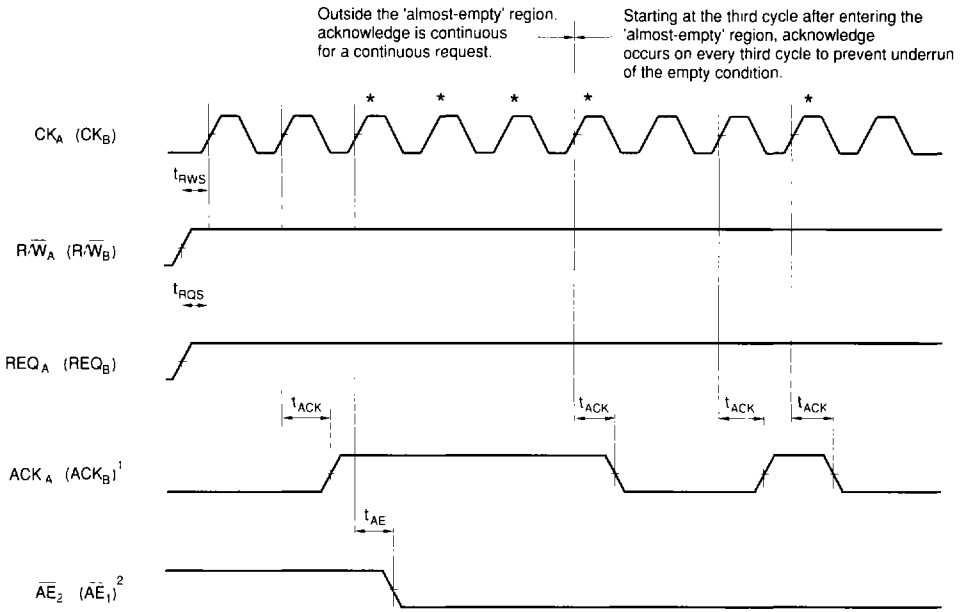
FIGURE 37. WRITE REQUEST/ACKNOWLEDGE HANDSHAKE



NOTES:

1. *For a FIFO access to occur, REQ and EN must be held HIGH for the required setup and hold times.*
2. ACK can be tied directly to EN to directly gate FIFO accesses.
   * Indicates where a write would take place, if ACK were tied to EN.
3. REQ must be maintained HIGH with R/$\overline{W}$ stable throughout entire clock cycle for ACK to be generated.
4. When the REQ/ACK handshake is not used, ACK can be ignored, and REQ may be tied HIGH or used as a second enable.
5. Parameters without parentheses apply to Port A. Parameters with parentheses apply to Port B.

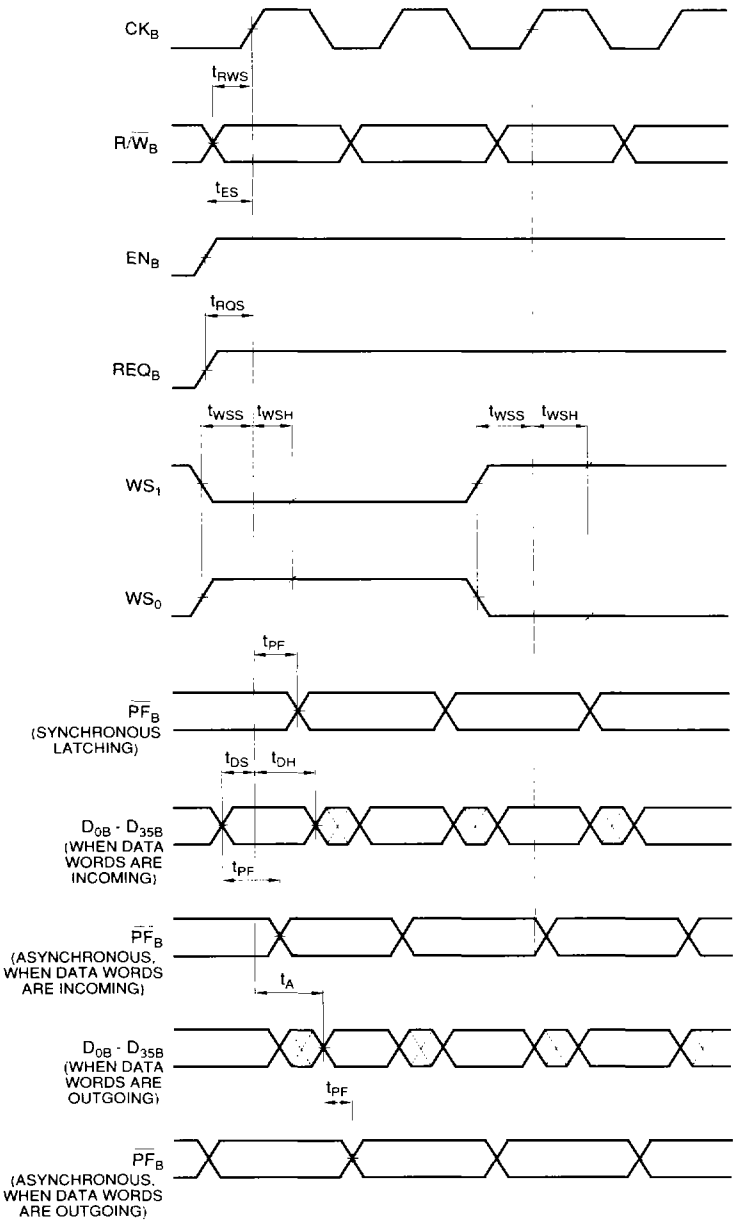
FIGURE 38. READ REQUEST/ACKNOWLEDGE HANDSHAKE



NOTES:

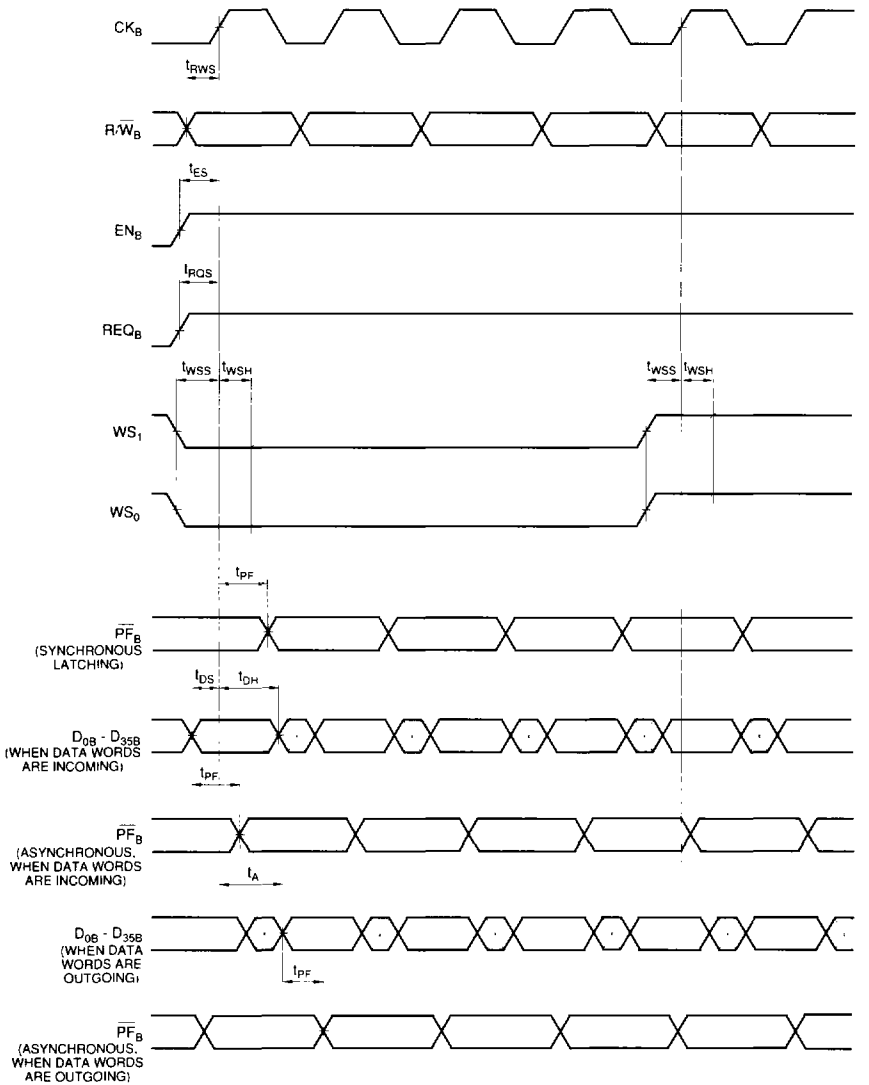
1. For a FIFO access to occur, REQ and EN must be held HIGH for the required setup and hold times.
2. ACK can be tied directly to EN to directly gate FIFO accesses.
   * Indicates where a read would take place, if ACK were tied to EN.
3. REQ must be maintained HIGH with R/W stable throughout entire clock cycle for ACK to be generated.
4. When the REQ/ACK handshake is not used, ACK can be ignored.
   and REQ may be tied HIGH or used as a second enable.
5. Parameters without parentheses apply to Port A. Parameters with parentheses apply to Port B.

FIGURE 39. CHANGING PORT B WORD-WIDTH SELECTION DURING OPERATION



NOTE: During retransmit, WS_1 and WS_0 must be stable throughout entire clock cycle.

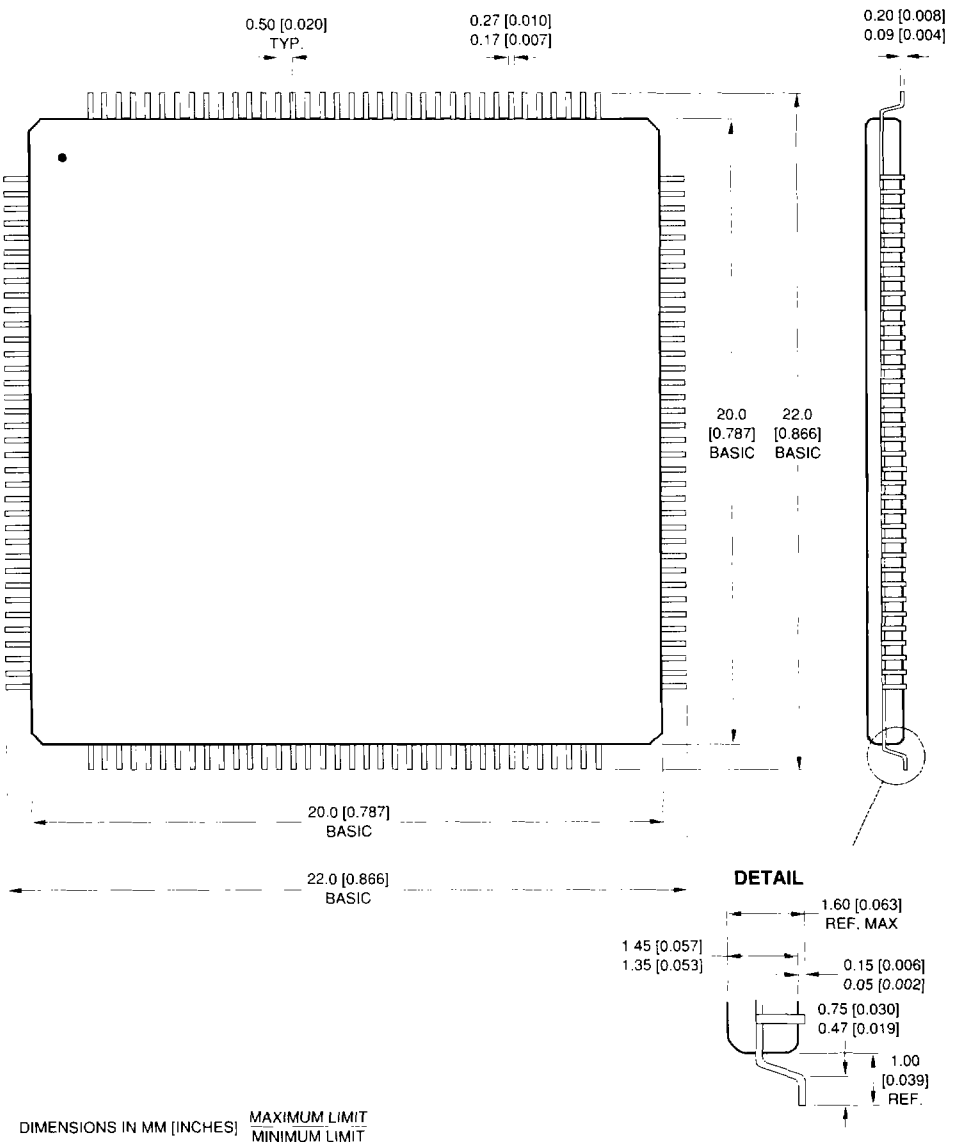
FIGURE 40. PARITY GENERATION



NOTE: During parity mode changes (odd or even), T_{PF} may have additional delay from the rising edge of the clock.

PACKAGE DIAGRAMS 144-PIN TQFP

144TQFP (TQFP-144-P-2020)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

ORDERING INFORMATION

Example: